

● MEM7A  
● ● MEM7B  
● ● ● MEMORY

M-4909  
(TD-4305)

TECHNICAL MANUAL

# MEMORY

## MEM7A      MEM7B



TD:4305

### ABSTRACT

This manual describes MDS Qantel's MEM7B Random Access Memory assembly and MEM7A parity checking and interface assembly. Included are: an overview of memory architecture, a gate-by-gate explanation of the MEM7A and MEM7B logic diagrams, Read, Write, and Refresh timing diagrams, and the timing sequencer PROM listing.



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## SECTION 1

## INTRODUCTION

### 1.1 GENERAL DESCRIPTION

The MEM7B memory card contains dynamic, random access, read-write, memory. Each MEM7B provides 131,072<sub>10</sub> memory locations (128K), each being 9 bits wide. The parity bit generated from each 8 bit data byte is stored on the MEM7B along with the data byte written to any memory location. Eight MEM7B cards may be mounted on each MEM7A board assembly, providing a maximum of 1,048,576<sub>10</sub> memory locations (1M). In hexadecimal, each MEM7B represents \$100000 locations (\$000000 through \$0FFFF) while a fully equipped MEM7A assembly with eight MEM7B cards represents \$1000000 locations (\$000000 through \$FFFFFF).\*

The MEM7B/MEM7A memory assemblies are employed by MDS Qantel systems having the Q30 or Q30R CPU. This includes all models of the System 40 series. It is also possible to upgrade the 200/300 Series Systems, 2X Series Systems, 1400 Series Systems, and 900 Series Systems for Q30 or Q30R operation by installing the proper backplane. For more information on the system upgrades refer to the Installation Instructions for the Q30 Enhancement Kits listed in the Related Documents Section.

The MEM7A includes parity generation/checking logic with the ability to interrupt the CPU in the event of a parity error. Under normal system operation true odd parity is kept. A parity bit of appropriate logic level is generated causing the 9 bits written in any memory location (8 bit data byte + parity bit) to contain an odd number of logically high bits. When a memory location is later addressed by a read operation, if the parity checking feature is enabled, parity is again calculated by presenting the parity generator inputs the 8 bit data byte

\*Dollar sign indicates hexadecimal notation

from RAM along with the stored parity bit read from memory. The parity generator should always find an odd number of logically high bits at this time. An even number of logically high bits presented to the parity generator during a read operation will generate a parity error signal. If the Interrupt and Indicator features are enabled, a parity fault interrupt signal is sent to the CPU and magnetic visual indicators (on both the MEM7A and the failing MEM7B) are set.

The MEM7A functions like an I/O controller, receiving control information from the backplane IOE bus. It responds to status inquiries, accepts write controls, and responds to reset I/O. The parity bit RAMs may be swapped with the RAMs normally designated to the least significant data bit. This permits full diagnostic testing of the MEM7B RAMs.

## 1.2 RELATED DOCUMENTS

The following is a list of MEM7B and MEM7A documents available from the MDS Qantel Drafting Department.

D32109	MEM7A Logics*
D32110	MEM7B Logics*
L51069	MEMTIME2 Timing PROM Listing*
A32142	Backplane Pin Listing, BP6S and BP6L
A52021	Design Spec., MEM7
A12737	IC 4164, 64K Dynamic RAM
A53029	Engn. Test Procedure, MEM7A/B

Installation instructions for the Q30 Enhancement Kits are available from the MDS Service Documentation Distribution office.

TD-4027	Upgrading 1400 Series Systems
TD-4028	Upgrading 2X Series Systems
TD-4029	Upgrading 900 Series Systems
TD-4030	Upgrading Series 200/300 Systems

\*These documents are reproduced in the Appendix of this manual.

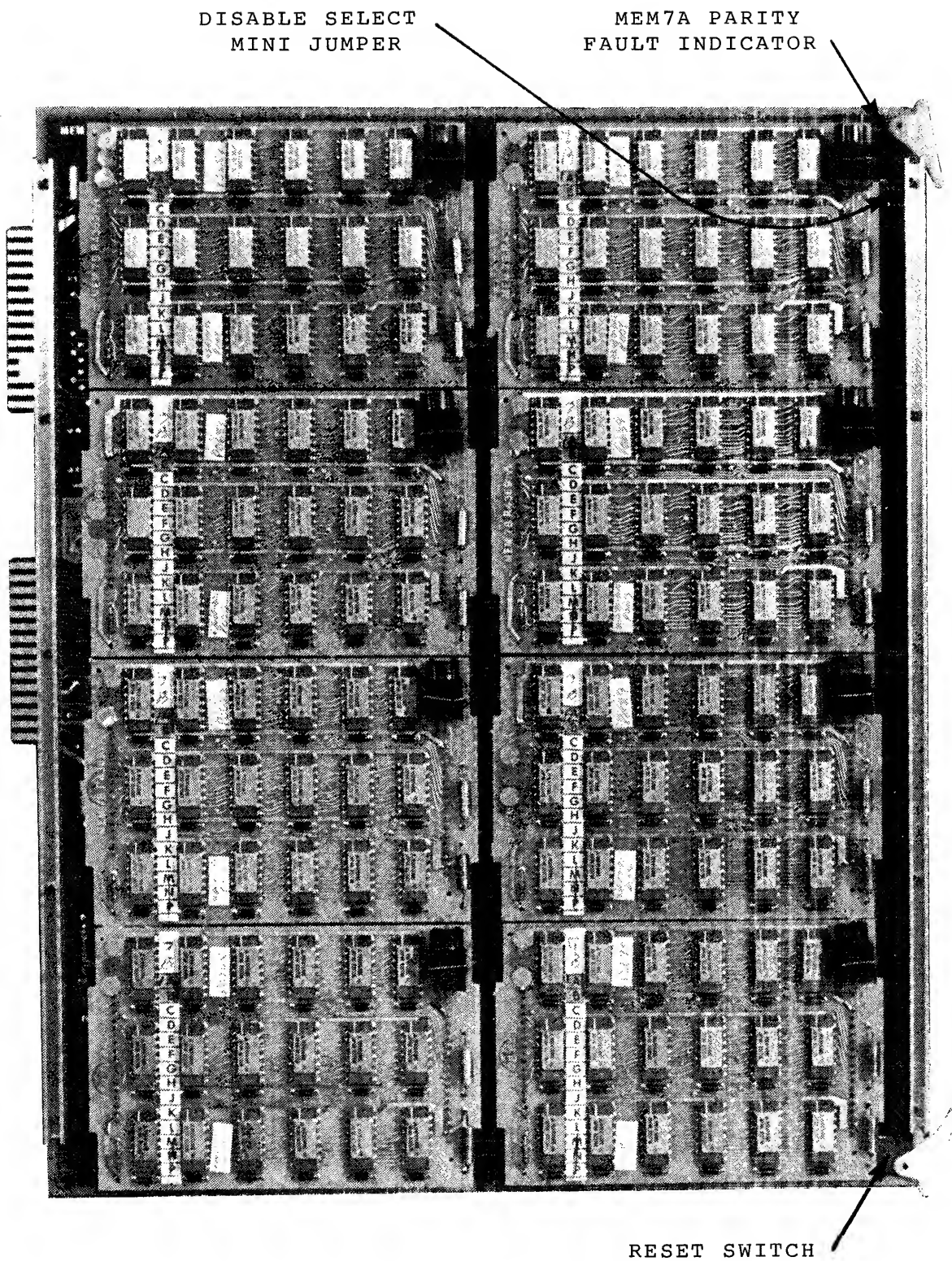


FIGURE 1-1  
MEM7A WITH 8 MEM7B CARDS

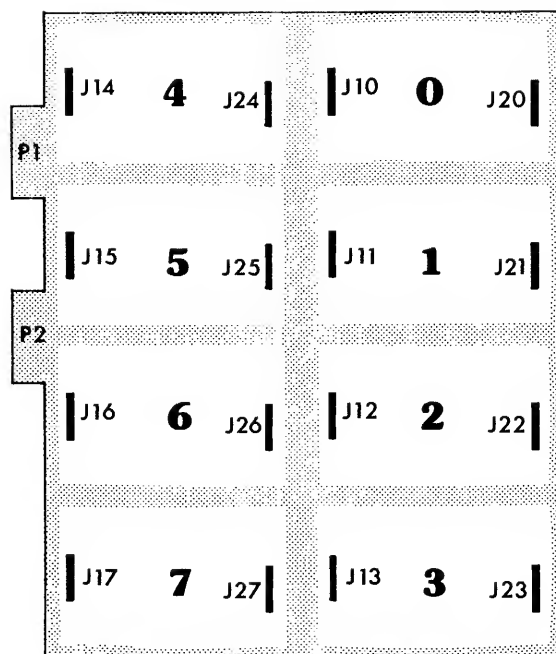


FIGURE 1-2  
MEM7B ORIENTATION

### 1.3 PHYSICAL DESCRIPTION

A MEM7A assembly carrying 8 MEM7B cards is shown in Figure 1-1. The MEM7B cards attach to the MEM7A by connectors J10 through J27 (see Figure 1-2) and are keyed to minimize incorrect insertion. Also shown in Figure 1-2, the relative positions for the MEM7B cards on the MEM7A are numbered, 0 through 7. As additional MEM7B cards are added to an unfilled MEM7A board the numerical order of the card positions must be followed to ensure continuity of memory.

The MEM7A parity fault indicator is pointed out in Figure 1-1. The indicator displays a fluorescent green color when a parity error is detected. Upon pulling the MEM7A assembly from the backplane,\* the MEM7B parity fault indicators (located in the upper right corner of each MEM7B) may be examined to determine which MEM7B card experienced the parity error.

\*Be sure power to the backplane is off when removing or inserting any boards.

The parity fault indicators consist of a permanently magnetized disc with one side painted black and the other side painted fluorescent green. The disc resides on two pivot points above an encapsulated coil. A detected parity error sends a current pulse through the coil causing a magnetic field whose polarity causes the magnetized disc to be repelled. This causes the disc to flip over and expose its fluorescent green side. The indicator disc can be flipped back to expose its black side by passing a current pulse through the coil in a direction opposite to the indicator setting current. The MEM7A has a reset pushbutton for clearing its parity fault indicator (see Figure 1-1). The parity fault flip flop on the MEM7A must be reset by a write control instruction to memory before depression of the reset pushbutton will affect the parity fault indicator.

The MEM7A responds to control signals from the backplane IOE bus. The device address for selecting the MEM7A is fixed at \$5.

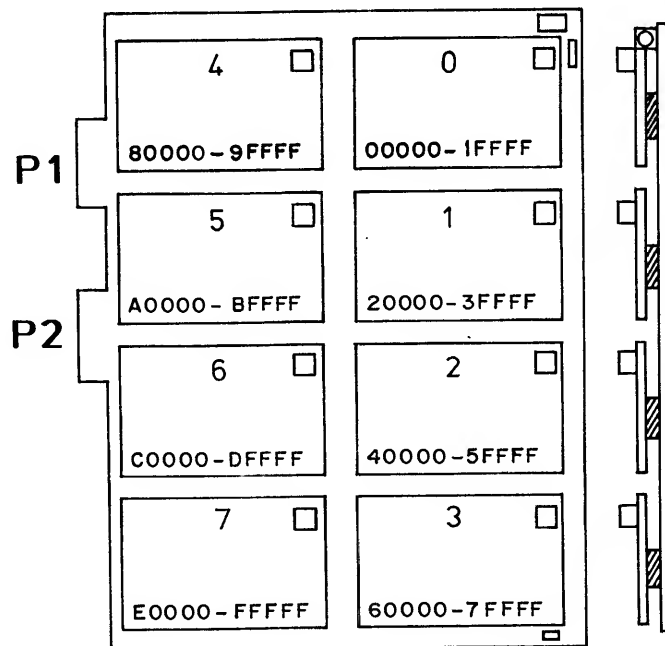


FIGURE 1-3  
MEM7B ADDRESS MAP

In all systems utilizing the Q30 or Q30R, the MEM7A/B assembly is installed in the backplane memory slot immediately to the left of the CPU slot. The 3 remaining memory slots will normally not have connectors installed (this backplane is also used for Q29 systems with MEM6AR/B assemblies). There are three jumpers on the backplane which must be in the proper position for the Q30 to address its MEM7A/B assemblies properly. See Figure 1-4 for the location and proper positioning of these soldered jumpers.

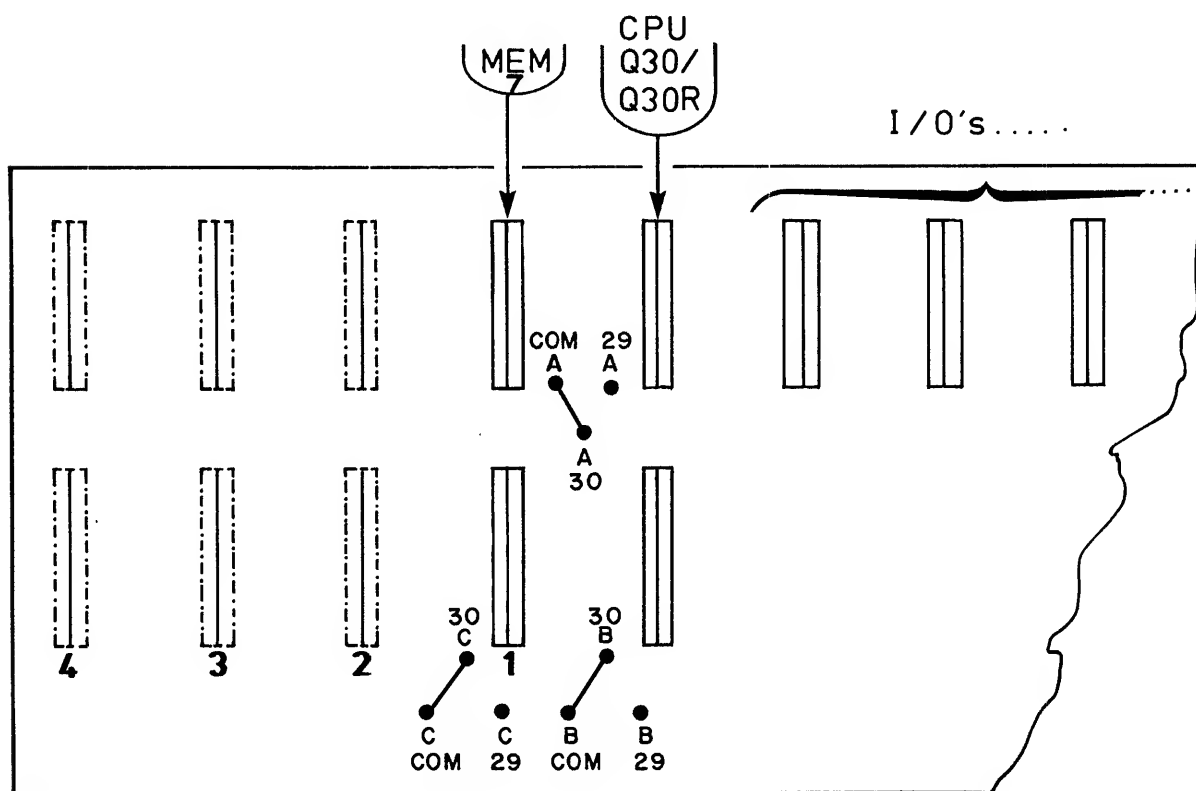


FIGURE 1-4  
BACKPLANE JUMPERS

The Disable Select mini-jumper (see Figure 1-1) must be installed for normal operation. If the cap of the mini-jumper is removed, the output of the Select flip flop can no longer enable the write control decoders on the MEM7A. At the repair center special test bed systems (with multiple MEM7 memory slots) are used, allowing the system to be bootstrapped on a known good MEM7A/B. This permits the technician to perform I/O and write control commands to a failing MEM7A/B assembly without disturbing the operating conditions of the known good MEM7A/B. An ATP program loaded into the known good memory can specify testing of specific blocks of memory on the failing MEM7A/B as well as issue write control and status request commands specifically directed to the MEM7A/B under test.

## SECTION 2

## MEM7 BASICS

### 2.1 MEMORY CHIP

The memory IC used on the MEM7B assemblies is a  $65,536_{10}$  location 1 bit wide, dynamic NMOS RAM. Pin designations and a block diagram of the chip's internal circuitry are given in Figure 2-1. A single supply voltage (+5V) is supplied to the  $V_{DD}$  terminal while the  $V_{SS}$  terminal serves as the ground connection.

All input and output signal levels involving the RAM follow TTL conventions. Internal latches are provided on the Data In, Data Out, and Address lines. Tri-State buffering is provided on the Data Out line.

The 16 bit address needed to specify one of 64K memory locations is multiplexed via 2 time states onto the 8 address inputs of the RAM. The internal memory cells are arranged in a row and column matrix. An 8 bit row address is first applied to the address inputs and latched into the chip by a logic low at the Row Address Strobe ( $\overline{RAS}$ ) input. An 8 bit column address is then applied and latched into the chip by a logic low at the Column Address Strobe ( $\overline{CAS}$ ) input.

During a write operation, Write Enable ( $\overline{WE}$ ) is sent active low before  $\overline{CAS}$  causing the Data Out line to remain in tri-state condition throughout the memory cycle. The input data is latched into the RAM's internal Data In latch on the negative-going transition of  $\overline{CAS}$  while  $\overline{WE}$  is low.

During a read operation, valid data will be present at the RAM outputs approximately 100nSec after  $\overline{CAS}$  goes active low.

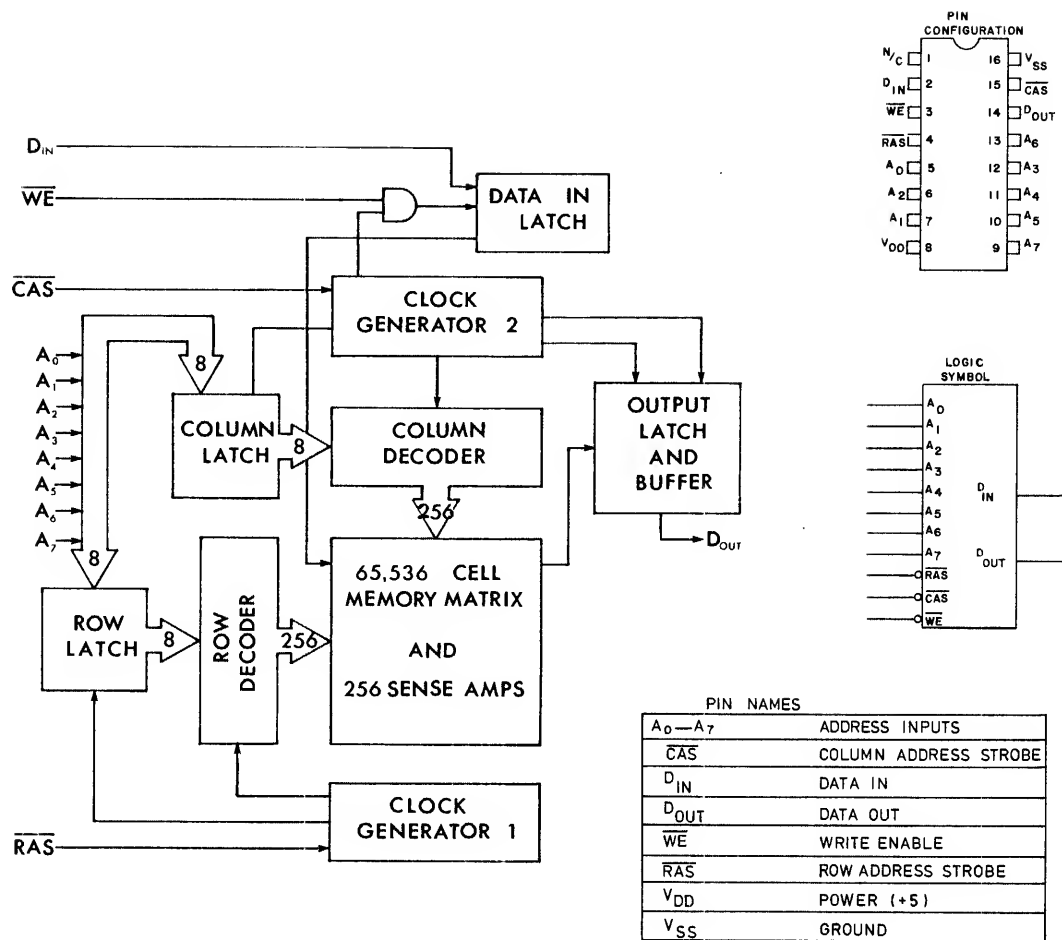


FIGURE 2-1  
MEMORY IC BLOCK DIAGRAM

The RAM chips must be refreshed within a 2mSec period to retain data. This is accomplished by strobing a unique 7 bit row address into the chip approximately every 14μSec. The refresh address and timing are generated and controlled by the CPU.

Eighteen RAM chips are employed on each MEM7B card. Each RAM is a 64K location memory, but is only 1 bit wide (e.g., a 64K/9 bit memory module would require nine of the 64K RAM chips with each chip storing all the information of one bit position in the memory word throughout the entire 64K locations). The 18 RAM chips on each MEM7B establish 128K locations of memory each 9 bits wide.

Two RAMs are dedicated to each bit position of the data byte as well as the parity data bit. The two 9 RAM, 64K memory modules on each MEM7B are designated as the L (lower) and U (upper) module. Each module receives a unique  $\overline{\text{RAS}}$  signal from the MEM7A timing sequencer.

The MEM7A decodes 4 backplane address bits and generates one of 16 RAS signals on a memory operation. On a refresh operation, all 16  $\overline{\text{RAS}}$  signals are generated simultaneously so the 7 bit refresh address is strobed into all the RAMs on the assembly.

## 2.2 MEM7B RAM DESIGNATIONS

Figure 2-2 orients the data bit/parity bit designations to their physical board location. For Example, Data Bit 06 is stored in the RAMs at 1C and 2C.\* The parity data bit is stored in the RAMs at 5C and 6C. The L and U module RAMs are specified in the Figure.

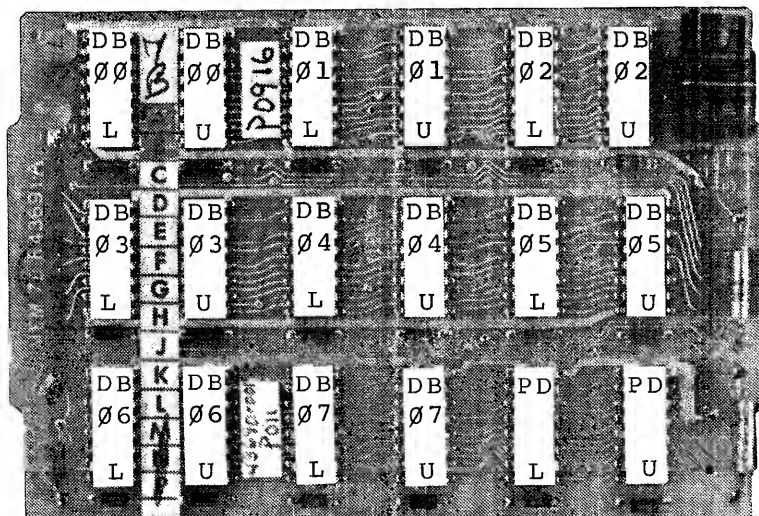


FIGURE 2-2  
MEM7B RAM DESIGNATIONS

\*The numerical reference defines vertical column (1-6), while the alphabetical reference defines horizontal row (A-C).

ADDRESS	MEM7B POSITION	64K MODULE
\$000000 - 0FFFFF	0	L
\$100000 - 1FFFFF		U
\$200000 - 2FFFFF	1	L
\$300000 - 3FFFFF		U
\$400000 - 4FFFFF	2	L
\$500000 - 5FFFFF		U
\$600000 - 6FFFFF	3	L
\$700000 - 7FFFFF		U
\$800000 - 8FFFFF	4	L
\$900000 - 9FFFFF		U
\$A00000 - AFFFFF	5	L
\$B00000 - BFFFFF		U
\$C00000 - CFFFFF	6	L
\$D00000 - DFFFFF		U
\$E00000 - EFFFFF	7	L
\$F00000 - FFFFFF		U

FIGURE 2-3  
MEMORY ADDRESS MAP

## 2.3 I/O COMMANDS

The MEM7A responds when the following I/O commands appear on the backplane E bus, providing a device select operation has selected device \$5. Any MEM7A with the DIS SEL (Disable Select) jumper removed will be disabled from performing all I/O commands except Reset I/O and System Reset. The DIS SEL jumper must be installed for normal operation.

CONTROL CODE	MNEMONIC	COMMAND
\$1	RSØ-N	Read Status Ø
\$3	WRC-N	Write Control
\$4	RIO-N	Reset I/O
\$9	RS2-N	Read Status 2

### 2.3.1 READ STATUS Ø

A Read Status Ø request to the MEM7A always receives an \$E4 response.

### 2.3.2 WRITE CONTROL

A Write Control instruction issued to memory (Device \$5) has the ability to establish the following control conditions;

- Enable Parity Checking
- Enable CPU Interrupts upon Parity Error
- Swap Parity and Data bit Ø RAMs
- Select Even Parity
- Reset Parity Error Flip Flop

The control byte sent via the backplane data bus to the memory write control register is coded as follows:

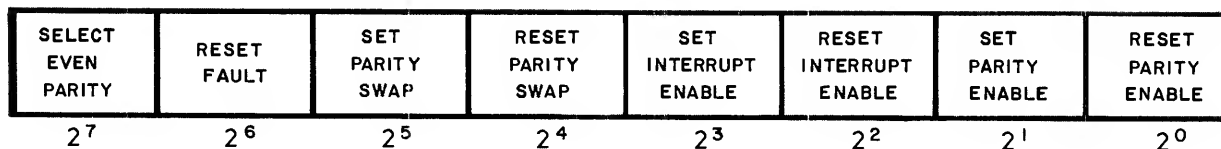


FIGURE 2-4  
WRITE CONTROL BYTE

Note, a separate bit position is provided to set or reset most of the write control conditions. This allows any control mode to be set or reset without affecting the state of the other bits in the write control register. With this arrangement the CPU doesn't need to interrogate the contents of the write control register before issuing a write control byte. The bit weight dedicated to each control of the write control byte is tabulated below:

\$01	Reset Parity Checking
\$02	Set Parity Checking
\$04	Reset Interrupt Enable
\$10	Reset Parity Swap
\$20	Set Parity Swap
\$40	Reset Parity Fault
\$80	Set Select Even Parity

A logic low on the \$80 weight bit sets odd parity, the condition used under normal operation.

### 2.3.3 RESET I/O

A Reset I/O instruction issued to memory (Device \$5) clocks reset the Parity Enable, Interrupt Enable, and Parity Swap flip flops of the write control register and directly resets the Select Even Parity flip flop and the Parity Error flip flop.

### 2.3.4 READ STATUS 2

If no parity error has occurred, a Read Status 2 request receives an \$F6 response from the MEM7A assembly. A Read Status 2 inquiry after a parity error specifies the physical position on the MEM7A of the failing MEM7B card (0-7) and the 64K module (L or U) on that MEM7B.

READ STATUS 2 CODE	MEM7B POSITION	64K MODULE
\$07	0	L
\$17	0	U
\$27	1	L
\$37	1	U
\$47	2	L
\$57	2	U
\$67	3	L
\$77	3	U
\$87	4	L
\$97	4	U
\$A7	5	L
\$B7	5	U
\$C7	6	L
\$D7	6	U
\$E7	7	L
\$F7	7	U

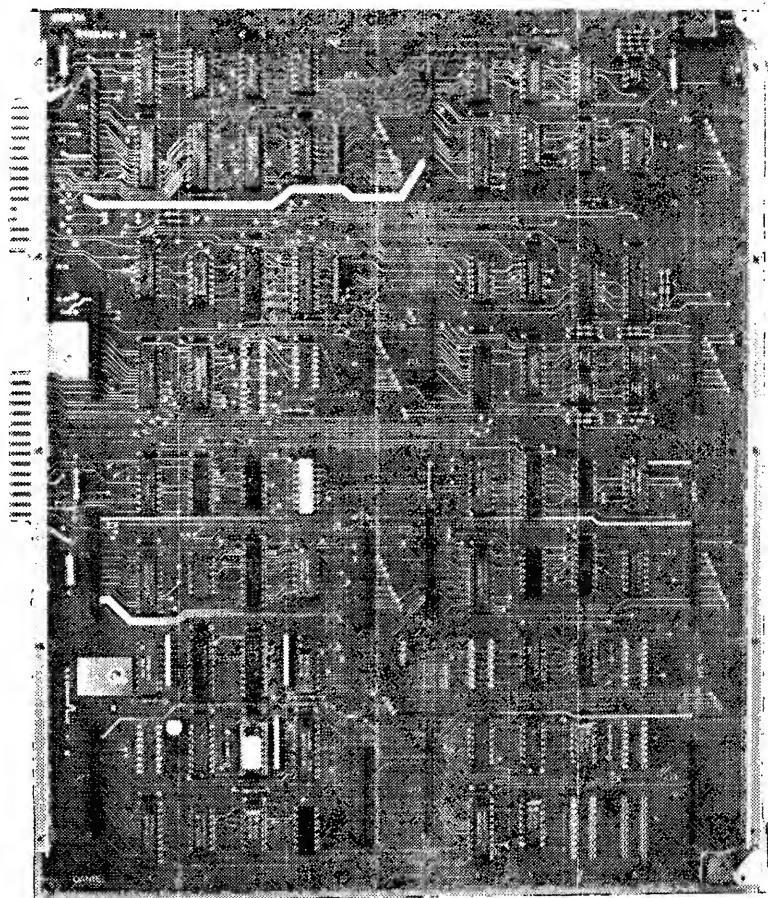


FIGURE 2-5  
MEM7A BOARD

## 3.1 LOGIC CONVENTIONS

This section presents a gate-by-gate explanation of the MEM7A and MEM7B hardware. The MEM7A logics (drawing No. D32109) and the MEM7B logics (drawing No. D32110) are referenced in a sheet by sheet manner. Throughout the section, integrated circuit devices are specified by their board location coordinates (as, the Parity Generator at 4B). A particular gate in an IC package is specified by its board location followed by the pin number of its principle output (as, the Nand gate at 5A-3).

When a circuit discussion references a component on a logics sheet different from the sheet currently under discussion, the different sheet number will precede the circuit location of the component. For example, (7)6A-6, the Select flip flop on Sheet 7.

The active state of signals on the logic drawings are indicated by the suffix following each signal name; -N indicating an active low signal, -P indicating an active high signal.

Section 3.2 lists and defines the signal acronyms used by the MEM7A and MEM7B logics. The remainder of this section comprises an in-depth description of the hardware. The specific schematics sheet number being discussed is given in capital letters at the top of each page. The MEM7A and MEM7B logics are reproduced on Z folded sheets in the Appendix of this manual.

### 3.2 SIGNAL ACRONYMS

AD7/0-P - AD13/6-P AD7/15-P	The least significant 8 bits of the backplane address bus. The Q30 multiplexes a 16 bit (64K) address onto this bus via 2 time states.
AD16-P - AD19-P	Four backplane address bits encoded to specify one of seven MEM7B cards and the upper or lower 64K RAM module on that MEM7B.
BAD16-P - BAD19-P	Bank Address bits generated by latching the AD16-P through AD19-P backplane address bits.
CAST-N	Column Address Strobe generated from the timing control logic on the MEM7A.
CASx-N	Column Address Strobe signals individually buffered for each MEM7B assembly. (x = 1 of 8)
CLHI-N	The 11MHz clock from the Q30 CPU
DA00-P - DA07-P	Backplane data bus
DB00-P - DB07-P	Internal data bus of the MEM7A routed to all the MEM7B cards.
DMCY-N	Dynamic Memory Cycle
DMWR-N	Dynamic Memory Write
INTENA-P	Interrupt Enable
IOE00-P - IOE04-P	I/O control bus from the Q30 CPU
LAD16-P - LAD19-P	Latched backplane address bits

xMA00-P - xMA07-P	One of 8 buffered memory address buses carrying the multiplexed address and refresh address to the MEM7B assemblies. (x = 1 of 8)
MR-N	Master Reset
MSTAS-N	Memory Status enable
MSTAT-N	Backplane memory status signal, indicates the memory cycle is complete.
NRD-N	Normal Read
NWR-N	Normal Write
PARFLT-N	Parity Fault status signal sent to the Q30
PARIND-P	Parity error indication signal from the parity error flip flop
PARSWAP-N	Parity swap signal causes the parity bit to be stored in the RAMs normally dedicated to the least significant data bit. The least significant data bit is then stored in the RAMs normally dedicated to the parity bit.
PD-P	Parity data bit generated and stored on each write operation. Later, it is read with the data on a read operation so error detecting parity calculation may be performed.
PENA-P	Parity enable signal permits a detected parity error to be recorded by the parity error flip flop.

PFLT-P	Parity fault signal from the parity generator
PUPx-P	Pull-up resistor x
RAS-N	Row address strobe signal from the MEM7A timing logic
RASAx-N	The decoded row address strobe signal routed to the lower (L) module of each MEM7B (x = 1 of 8)
RASBx-N	The decoded row address strobe signal routed to the upper (U) module of each MEM7B (x = 1 of 8)
RDD-N	Read signal generated by the absence of a write or refresh operation.
RDL-N	Read latch signal from the MEM7A timing logic, clocks the parity error flip flop
RESFLT-N	Reset fault bit from the write control register
RF-N	Backplane refresh signal
RFSH-N	Refresh signal from the mode select latch
RIO-N	Reset I/O signal decoded from the IOE bus
RSØ-N	Read status Ø signal decoded from the IOE bus
RS2-N	Read status 2 signal decoded from the IOE bus

SELEVENPAR-N	Select even parity bit from the write control register
SETINDx-N	The drive signal which sets the parity error indicator on the selected MEM7B card. (x = 1 of 8)
SRD-N	Swapped read
STROBE-N	Strobe signal from the backplane
SWR-N	Swapped write
SYSRES-N	System reset signal from the backplane
WR-N	Write signal from the MEM7A timing control logic
WRC-N	Write control signal decoded from the IOE bus
WRD-N	Write data signal from the mode select logic
WRTx-N	The individual write line to each MEM7B card (x = 1 of 8)

### 3.3 DATA BUS BUFFERS

The data input latch at 3B is a tri-state transparent latch. The data output buffer at 2B is an octal tri-state buffer. These chips provide the bidirectional buffering between the backplane data bus DA00-P through DA07-P and the data bus common to all MEM7B cards on the MEM7A, DB00-P through DB07-P.

The outputs of Latch 3B are released from tri-state mode when an active low WRD-N (Write Data) and RAS-N (Row Address Strobe, from the MEM7A timing sequencer) are present at 6B-4. This drives 6B-1 logically low providing the output enable to pin 1 of latch 3B. CAST-N (Column Address Strobe, from the MEM7A timing sequencer) controls the functioning of the latch. When CAST-N is inactive (logically high) the latch at 3B is transparent and data at its inputs is gated directly to its outputs (providing the chips tri-state output buffer is enabled). When CAST-N drops logically low the data present at the inputs is latched into 3B and held until CAST-N returns to the inactive state (high). The latch at 3B also serves as a holding register, providing the input data to the inputs of the parity generator at 4B.

During a read operation, the active low RDD-N (Read Data) and RAS-N (Row Address Strobe) drive Negative-Nand gate 6B-10 high, generating a low from 6B-13 which enables the tri-state buffer at 2B. Read data which the selected MEM7B is outputting onto the DB00-P through DB07-P bus is thus enabled onto the backplane data bus DA00-P through DA07-P.

### 3.4 PARITY GENERATOR

During a write operation, the Parity Generator at 4B receives the write data byte latched into 3B. Notice, the ninth input to the

parity generator 4B-4 is pulled high by a pull-up resistor as parity is being generated during each write operation. Odd parity is normally kept by the MEM7 memory. SELEVENPAR-N (Select Even Parity) may be set active low (for diagnostic purposes) by a write control instruction to memory. A low SELEVENPAR-N will pull down pin 4 of the parity generator via the tri-state buffer 7C.

During a read operation, the data byte and parity bit are presented to the parity generator inputs from the RAMs outputs (data bit 0 and the parity bit are routed via the tri-state buffers at 8C). A logically low parity bit read from a location will pull down the ninth input of the parity generator 4B-4.

### 3.5 MODE SELECT MULTIPLEXERS

NWR-N (Normal Write) from the mode select logic enables pin 19 of 7C causing the odd parity output of the parity generator to be routed to the parity RAMs via the PD-P line. Also, the least significant data bit from the data input latch is routed onto the DB00-P line. During a swapped write operation, SWR-N (from the mode select logic) enables pin 1 of 7C causing the output of the parity generator to be routed onto the DB00-P line. Likewise, the least significant data line from the data input latch 3B-2 is routed onto the PD-P line.

During a Normal Read operation, NRD-N enables pin 1 of 8C enabling the output of the accessed parity RAM onto the ninth input of the parity generator 4B-4 and enabling the DB00-P line from the RAMs onto the least significant data bit position of the tri-state output buffer at 2B-2. A Swapped Read operation sends an active low SRD-N from the mode select logic to enable

MEM7A

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pin 19 of 8C. This multiplexes the contents of the RAMs normally used to store the parity bit onto the least significant data bit of the output data bus and places the output of the RAMs normally storing the least significant data bit onto the ninth input of the parity generator 4B-4.

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### 3.6 ADDRESS LATCHES

The 8 address latches are illustrated on Sheets 2 and 3. The latches provide the necessary fanout drive for the multiplexed backplane address bus AD7/0-P through AD7/15-P, which must address 144 RAMs on a fully loaded MEM7A assembly (with 8 MEM7B cards). Therefore, one address latch is provided to drive the 18 RAM chips on each of the MEM7B cards. The number prefixing each individual latched address bus corresponds with the numbering of the MEM7B card positions shown in Figure 1-2.

Pin 1 of all the address latches is hardwired to ground. The latch outputs are permanently enabled and never enter tri-state mode. The latches are controlled by the ADL-N (Address Latch) signal from the timing sequencer logic. When ADL-N is inactive (logically high) the latches are transparent. The negative-going transition of ADL-N latches the contents of AD7/0-P through AD7/15-P into all 8 address latches simultaneously.

### 3.7 MODULE SELECT

The Bank Address bits BAD16-P through BAD19-P are buffered versions of the backplane address bits AD16-P through AD19-P. The octal decoders at 2E and 7F generate 16 specific Row Address Strobe (RAS) signals by decoding the BAD16-P through BAD19-P address lines. The 16 Negative-Nor gates shown across the center of sheet 4 are normally enabled by a high from 8F-1 except during refresh operations. The tri-state buffers at 3F and 6E are permanently enabled. During a read or write operation, one of 16 RAS signals will be decoded by 2E and 7F and sent via the tri-state buffers to the appropriate 64K RAM module (L or U) on the appropriate MEM7B.

RFSH-N (Refresh) is generated when RF-N (the backplane refresh signal from the CPU) is latched into the MEM7A by the negative-going transition of RAS-N from the timing sequencer logic. The combination of the active low RFSH-N and RAS-N at Negative-Nand 8F-4 drives 8F-1 logically low forcing the outputs of all 16 Negative-Nor gates logically high. Thus, all 16 Row Address Strobe signals are generated during a refresh operation. The 100 ohm resistors on the outputs of the tri-state buffers help to reduce ringing.

### 3.8 CAS BUFFERS

The CAST-N signal (Column Address Strobe, from the timing sequencer logic) is buffered by the dual 4 bit tri-state buffers at 2H and 3H. This provides 8 simultaneous CAS signals, one for each MEM7B card (0 through 7). The output enable inputs (pins 1 and 19) of the tri-state buffers are hardwired to ground causing

MEM7A

SHEET 5

the outputs to be permanently enabled. The 100 ohm resistors help to reduce ringing. It is the decoded RASx-N signal that specifies which particular MEM7B card is to be accessed.

### 3.9 WRITE BUFFERS

WR-N (Write) from the timing sequencer logic is buffered by the remaining halves of the dual 4 bit tri-state buffers at 2H and 3H. The output enable inputs (pins 1 and 19) are hardwired to ground, permanently enabling the outputs of the tri-state buffers. During a write operation, the WR-N signal is fanned out providing 8 simultaneous WRTx-N (Write signal to MEM7B, x specifies MEM7B card, 0 through 7). The 100 ohm resistors help to reduce ringing.

SHEET 6

### 3.10 TIMING SEQUENCER

All the important timing signals for the MEM7A are generated from the timing sequencer logic shown at the right side of sheet 6. Basically, the circuit consists of the address counter 2J, programmed ROM 3J, and the pipeline register 4J.

The outputs from address counter 2J step the PROM through its sequences while the signals sent to pins 13 and 14 specify the sequence type (read, write, or refresh) and modify the duration of the outputted control signals accordingly.

When MR-N (Master Reset) is inactive, Nand gate 2K-6 is enabled. When an active low DMCY-N (Dynamic Memory Cycle) from the CPU drives 4K-6 high, the positive-going transition (from 4K-6) clocks flip flop 3K-5 set. This drives Nand gate 2K-6 low which

enables (via Negative-Nor gate 2K-8) the address counter 2J, initiating a sequencer timing cycle. RF-N (Refresh signal from the backplane) can directly set flip flop 3K-5 and likewise enable address counter 2J to initiate a sequence. Whenever flip flop 3K-5 is set, the outputs of the timing PROM 3J are enabled by 3K-6.

The active low RF-N will directly set flip flop 3K-9 sending a high to pin 13 of the PROM 3J, causing the sequence to generate a refresh timing sequence. The low from 3K-8 generates an enable to the address counter via Negative-Nor gate 2K-8. Flip flop 3K-9 is clocked reset by the positive-going trailing edge of the RAS-N signal.

When an active low DMWR-N (Dynamic Memory Write) enters from the backplane, flip flop 6K-9 is directly set. This sends a high to pin 14 of the PROM 3J causing the sequencer to generate a write operation timing sequence. The low from 6K-8 generates WRD-N (Write Data) for the mode select logic. Flip flop 6K-9 is clocked reset by the positive-going trailing edge of RAS-N.

CLHI-N (11MHz clock from the CPU) clocks both the address counter 2J and pipeline register 4J. The positive-going transition of CLHI-N loads the outputted data from the PROM into the pipeline register and simultaneously clocks the address counter causing it to increment. Incrementing the counter at this time does not affect the data being loaded into the pipeline register because a finite period of time passes before the counter's outputs assume the incremented state and the newly accessed PROM location propagates to the outputs of the PROM.

A feedback line from the pipeline register 4J-6 is routed to the synchronous reset input of address counter 2J and to the direct reset input of flip flop 3K-5. A low from 4J-6 signals the end of a sequence and provides an intelligent means of resetting the sequencer logic at the end of any memory timing operation. Another feedback line from the pipeline register 4J-9 enables the address counter 2J via Negative-Nor gate 2K-8.

Flip flops 6K-5 and 7J-9 are both clocked by the inverted CLHI-N signal from 4K-8 and generate the master RAS-N and CAST-N respectively. The sequencer initiates a row address strobe by generating a low from 4J-19 which directly resets 6K-5 and holds it directly reset until 4J-19 returns to a logic high state, allowing the next positive-going transition of CLHI to clock 6K-5 set.

CAST-N is generated from the flip flop 7J-9 when the timing sequencer generates a low from 4J-5, directly resetting 7J-9. After the direct reset from 4J-5 is lifted, a high from 4J-2 will cause the next positive-going transition of the CLHI signal from 4K-8 to clock flip flop 7J-9 set.

The microcode listing for the MEMTIME2 PROM at 3J is included in the Appendix of this manual.

## 3.11 ERROR INDICATOR DRIVERS

When a parity error is detected, the Parity Error flip flop is clocked set generating an active low PARIND-N signal. The negative going PARIND-N latches the present state of the BAD16-P through BAD19-P address bits into the latch at 2C. The latched bits LAD16-P through LAD19-P then are used to specify one of sixteen 64K memory banks (specifying the MEM7B and the upper or lower memory module on that MEM7B), pinpointing where the parity error occurred. If INTENA-P (Interrupt Enable) has been set in the MEM7A write control register it will provide an enable signal to the octal decoder at 6D. This allows PARIND-P to fully enable 6D and cause the BAD17-P through BAD19-P address lines to be decoded by the octal decoder. Thus, an active low set indicator signal is generated to the proper MEM7B. Non-inverting power drivers capable of sinking enough current to set the magnetic indicators are provided at the outputs of the octal decoders.

## SHEET 7

## 3.12 SELECT LOGIC

The inverting tri-state buffer at 1A receives the backplane IOE bus and the Strobe signal. The And gate at 4A-6 is driven logically high by an \$5 code on the IOE bus (the IOE bus is Negative true, an \$F code would drive all four IOE lines active low). The gates at 5A-8, 5A-6, 4A-8 are arranged to apply a high to the D input of the Select flip flop 6A-6 when a \$5 is present on the lower four bits of the backplane data bus. During a memory select operation the CPU presents an \$F on the IOE bus, a \$05 on the data bus, and the Strobe signal to memory and all I/O controllers in the system. The combination of an \$F on

the IOE bus and the Strobe drive Nand gate 5A-3 low. The positive-going trailing edge of STROBE-N causes 5A-3 to make its positive-going transition clocking the Select flip flop 6A-6. All other I/O controllers are clocked reset as the MEM7A (Device \$5) is selected. Note, SYSRES-N (System Reset) directly resets the Select flip flop at power-up or soft IPL.

The I/O command decoders are located at 2A and 3A. The Select flip flop must be set to provide the active low enable to pin 5 of the octal decoders. A DIS SEL (Disable Select) jumper is provided, removing this mini-jumper cap permanently disables the I/O command decoders 2A and 3A. Only MEM7A assemblies with the DIS SEL jumper installed will respond to control and status commands. However, data storage or retrieval is not affected by the removal of the DIS SEL mini-jumper.

### 3.13 COMMAND DECODERS

The octal decoder at 2A decodes a \$3 (WRC-N, Write Control) and \$4 (RIO-N, Reset I/O) on the IOE bus. As well as requiring enable signals from the Select flip flop (via the DIS SEL jumper) and the inversion of the IOE04 line, the Strobe signal provides the final enable to 2A and gates the duration of the WRC-N and RIO-N signals.

The octal decoder at 3A decodes a \$1 (RS0-N, Read Status Zero) and a \$9 (RS2-N, Read Status Two) on the IOE bus. The inversion of IOE02-N is used as an enable signal. The inversion of IOE04-N is routed to the most significant select input of 3A causing RS2-N (\$9) to be generated from the \$5 output of the decoder 3A.

## 3.14 WRITE CONTROL REGISTER

During a Write Control instruction to memory, decoder 2A generates WRC-N which enables the present contents of the backplane data bus through the tri-state buffer at 4C. The bits of the write control register formed by flip flops 5C and 6C are set and reset, in most cases, by separate bits of the write control byte. This allows any bit to be changed without affecting the state of the other bits of the write control register.

When set, 6C-9 enables an error signal from the parity generator to cause the parity error flip flop to be clocked set. When set, 6C-5 enables the output of the parity error flip flop onto the backplane interrupt line and enables the magnetic indicator decoder-driver logic. When flip flop 5C-9 is set, the data bit 0 line is swapped with the parity data line. Flip flop 5C-9 is reset under normal operation.

The \$40 weight bit of the write control byte is used to directly reset the parity error flip flop with the signal RESFLT-N. Flip flop 5C-6, when set, causes even parity to be generated by changing the state of the ninth input to the parity generator. Under normal system operation, 5C-5 is reset causing odd parity to be generated.

The trailing edge of RIO-N or SYSRES-N clocks flip flops 5C-9, 6C-5, and 6C-9 causing them to go reset. Also, 5C-6 is directly reset by an active low RIO-N or SYSRES-N.

## 3.15 STATUS OUT LOGIC

During a Read Status 0 instruction, RS0-N goes active low enabling the hardwired lows at 3C-13, 11, 15, and 17 through the tri-state buffer 3C. This causes 4 of the data bus lines to be pulled low. The other data bus lines are not pulled down and appear as logic highs. This generates an \$E4 response on the data bus. However, if parity checking has been enabled and a parity error has set the parity error flip flop, PARIND-N enabled by RS0-N will drive 6H-1 low enabling AD18-P, AD19-P, and a hardwired low (1C-10) onto the DA06-P, DA07-P, and DA05-P lines respectively. Thus, the upper nibble of the Read Status 0 byte will contain AD18-P and AD19-P in its 2 most significant bits.

A Read Status 2 instruction sends RS2-N logically low enabling PARIND-N onto the DA03-P line and a hardwired low onto the DA00-P line via the tri-state buffer 1C. If no parity error has been detected, 3C-1 remains high and the upper 4 bits of 3C (DA04-P through DA07-P) remain in tri-state mode. Thus, a normal (no parity error) Read Status 2 response is \$F6 (PARIND-N does not pull down the DA03-P line). If parity checking has been enabled and a parity error has set the Parity flip flop, PARIND-N will cause 6H-4 to go low during a Read Status 2 instruction, enabling the Latched address bits (LAD16-P through LAD19-P) onto the data bus (DA04-P through DA07-P), specifying the error location down to the MEM7B and 64K RAM module (U or L).

## 3.16 MODE SELECT LOGIC

RDD-N (Read) is generated from Nand gate 7B-6 as the absence of WRD-N (Write) and RFSH-N (Refresh).

Under normal operation, PARSWAP-N is inactive (logically high, indicating the parity swap feature is not being used). This enables the inversion of WRD-N at 8B-11 to generate NWR-N (Normal Write) from 7B-11. Likewise, the absence of WRD-N (logically high) generates NRD-N (Normal Read) from 8B-3.

During parity swap mode, PARSWAP-P is logically high enabling 8B-8 and 7B-3, permitting SRD-N (Swapped Read) and SWR-N (Swapped Write) to be generated respectively.

### 3.17 UPPER ADDRESS BUFFERS

The transparent latch at 2D receives AD16-P through AD19-P from the backplane and generates the Buffered Address lines BAD16-P through BAD19-P. When RAS-N is inactive the latch is transparent. When RAS-N drops active low the present state of the AD16-P through AD19-P bus is latched into 2D. The tri-state outputs of 2D are permanently enabled by the hardwired low at 2D-1.

### 3.18 PARITY ERROR STATUS BIT

The Parity Error flip flop 6A-9 is clocked each Read operation by the RDL-n (Read Latch) signal from the timing sequencer. Providing that parity checking has been enabled, a PFLT-P (parity Fault) signal drives 7A-11 high allowing the negative-going transition of RDL-N (via inverter 7A-6) to clock 6A-9 set. Once 6A-9 is in the set condition, the low from 6A-8 latches the flip flop in the set state until it is directly reset. A MR-P (Master Reset, generated by RIO-N or SYSRES-N) or a RESFLT-N (Reset Fault) signal from the write control register will directly reset the parity error flip flop 6A-9.

## MEM7A

### SHEET 9 CONTINUED

If the Interrupt Enable signal, INTENA-P, has been set (in the write control register) and a parity error has set the flip flop 6A-9, Nand gate 7A-8 is driven low. This causes power driver 8A-3 to go low providing a current sink path for the series circuit containing R13, C5, and the MEM7A parity error indicator. This causes the indicator to change into the error state (fluorescent green). The low from 7A-8 sends 7A-3 high, enabling a hardwired low through the tri-state buffer at 1E-6. This generates PARFLT-N, the parity error signal sent (via the backplane) to interrupt the CPU.

After the Parity Error flip flop has been reset, the magnetic indicator can be returned to the normal (black) state by use of the reset switch at 8K.

MSTAS-N (Memory Status) from the timing sequencer enables tri-state buffer 1E-3 sending an active low MSTAT-N onto the backplane. The positive-going, trailing edge of MSTAT-N indicates to the CPU that the memory operation is complete.

## MEM7B SHEETS 1 AND 2

### 3.19 MEM7B LOGICS

The MEM7B cards hold 18 RAM chips. The 8 bit multiplexed address bus MA00-P through MA07-P (which is buffered on the MEM7A) is routed in parallel to all the RAM chips. The WRT-N (Write) and CAS-N (Column Address Strobe) signals are also routed to all 18 RAM chips simultaneously. It is the decoded Row Address Strobe signal that selects a specific 64K RAM module. Therefore, RASA-N (Row Address Strobe, Lower 64K module) is routed to one set of 9 RAM chips, while, RASB-N (Row Address Strobe, Upper

64K module) goes to the remaining 9 RAM chips. Notice, pairs of RAM chips have their data input and output lines in common. Each pair is dedicated to store all the information for a specific bit position on the buffered MEM7A data bus (DB00-P through DB07-P).

An onboard reset button is not provided on the MEM7B to reset the parity error indicator. An indicator reset circuit is given below.

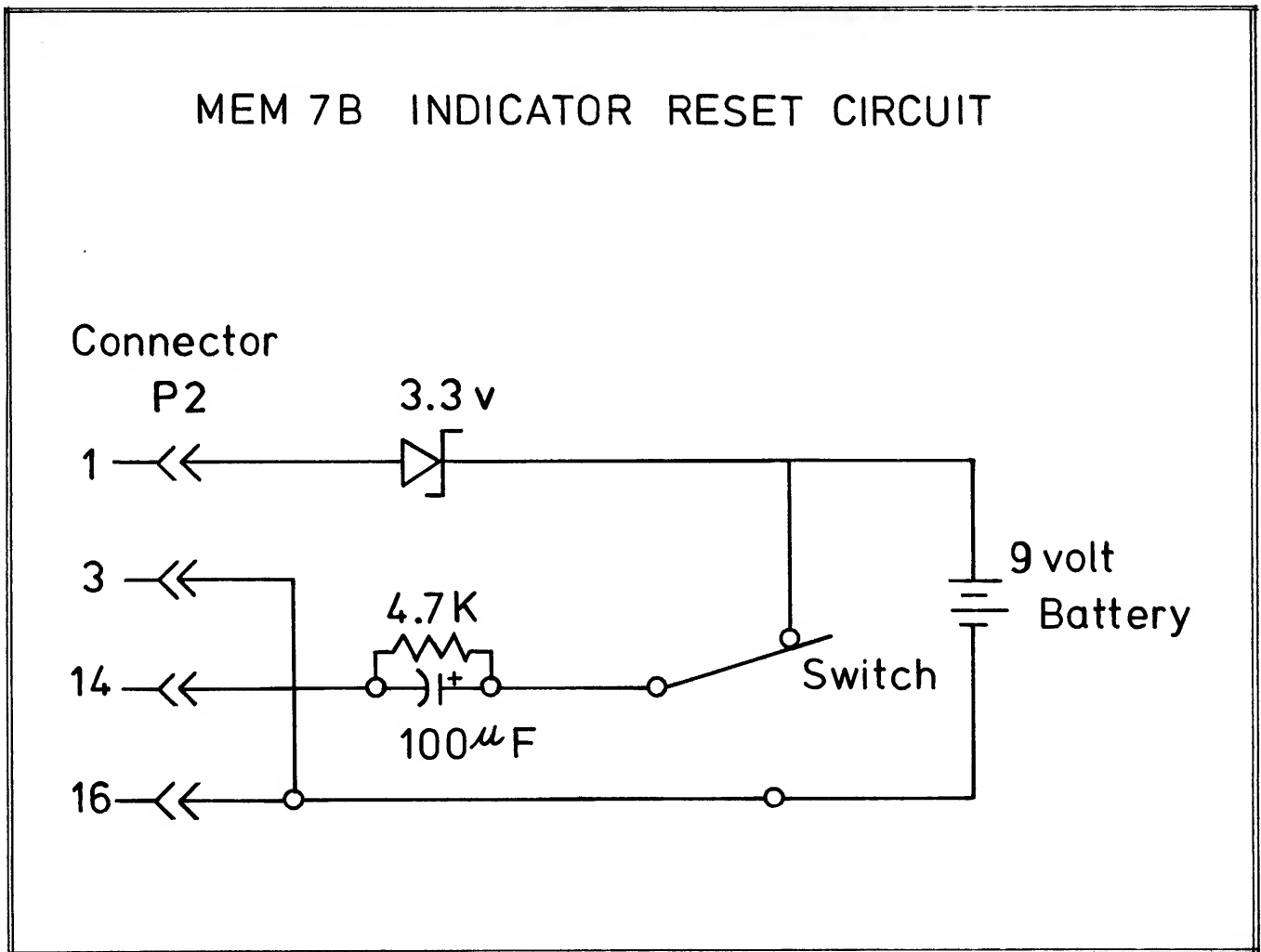
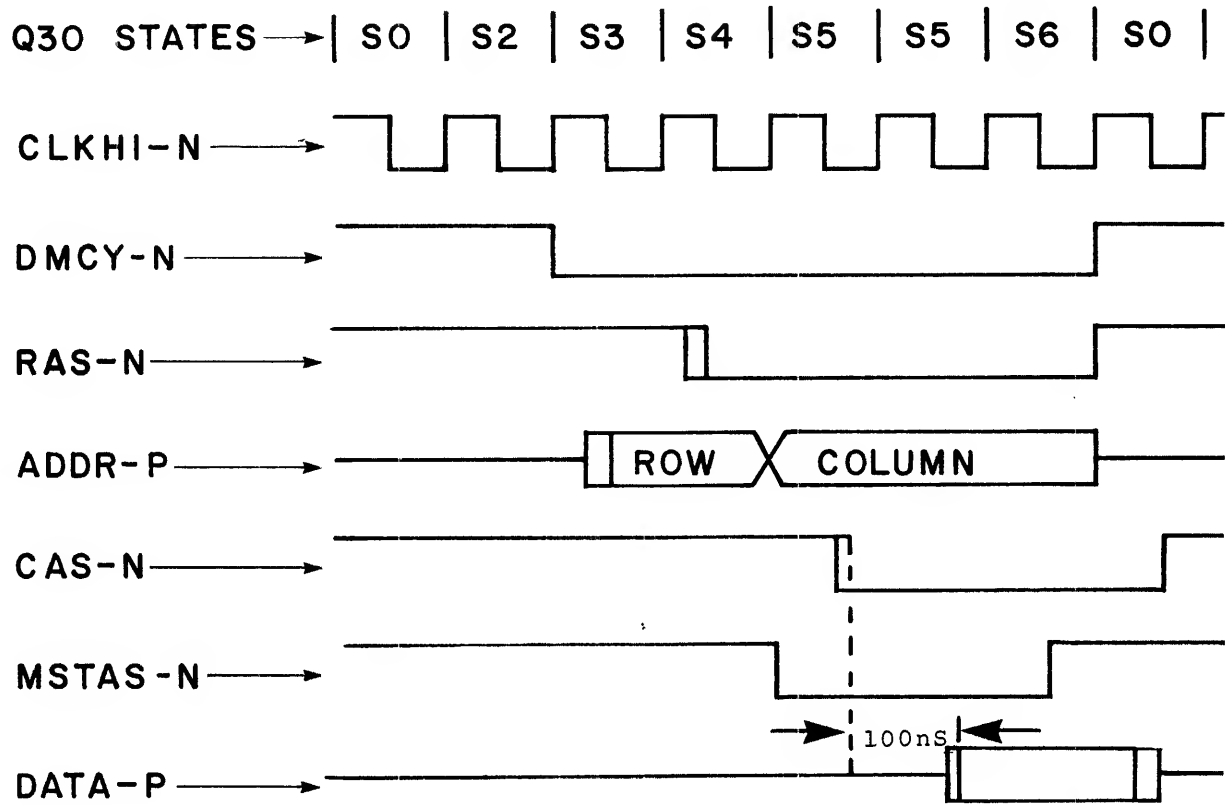


FIGURE 3-1

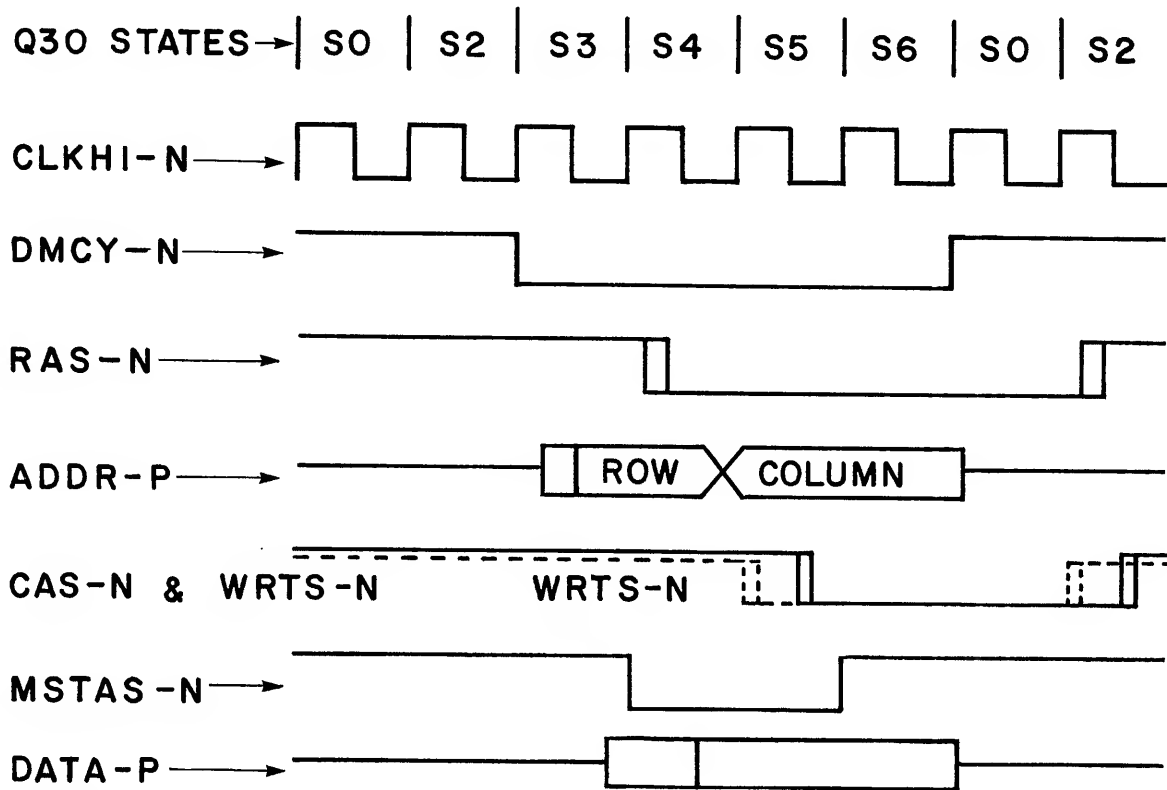
MEM7B INDICATOR RESET CIRCUIT

	3J-14	3J-13	10 3J-11 12	MEM7A TIMING PROM "MEMTIME2"								
ADDR	WR	RF	STATE	DATA	ENA	RDL	RES	MSTAS	ADS	WR	SCAS	RAS
0	0	0	000	F6	1	1	1	1	0	1	1	0
1	0	0	001	64	0	1	1	0	0	1	0	0
2	0	0	010	64	0	1	1	0	0	1	0	0
3	0	0	011	74	0	1	1	1	0	1	0	0
4	0	0	100	9F	1	0	0	1	1	1	1	1
5	0	0	101	DF	1	1	0	1	1	1	1	1
6	0	0	110	DF	1	1	0	1	1	1	1	1
7	0	0	111	DF	1	1	0	1	1	1	1	1
8	0	1	000	E7	1	1	1	0	0	1	1	1
9	0	1	001	76	0	1	1	1	0	1	1	0
A	0	1	010	56	0	1	0	1	0	1	1	0
B	0	1	011	DF	1	1	0	1	1	1	1	1
C	0	1	100	DF	1	1	0	1	1	1	1	1
D	0	1	101	DF	1	1	0	1	1	1	1	1
E	0	1	110	DF	1	1	0	1	1	1	1	1
F	0	1	111	DF	1	1	0	1	1	1	1	1
10	1	0	000	E6	1	1	1	0	0	1	1	0
11	1	0	001	60	0	1	1	0	0	0	0	0
12	1	0	010	70	0	1	1	1	0	0	0	0
13	1	0	011	DF	1	1	0	1	1	1	1	1
14	1	0	100	DF	1	1	0	1	1	1	1	1
15	1	0	101	DF	1	1	0	1	1	1	1	1
16	1	0	110	DF	1	1	0	1	1	1	1	1
17	1	0	111	DF	1	1	0	1	1	1	1	1
18	1	1	000	DF	1	1	0	1	1	1	1	1
19	1	1	001	DF	1	1	0	1	1	1	1	1
1A	1	1	010	DF	1	1	0	1	1	1	1	1
1B	1	1	011	DF	1	1	0	1	1	1	1	1
1C	1	1	100	DF	1	1	0	1	1	1	1	1
1D	1	1	101	DF	1	1	0	1	1	1	1	1
1E	1	1	110	DF	1	1	0	1	1	1	1	1
1F	1	1	111	DF	1	1	0	1	1	1	1	1
PROM (3J) output pin:					9	7	6	5	4	3	2	1
Pipeline Register(4J) pin:					9	12	6	15	5	16	2	19

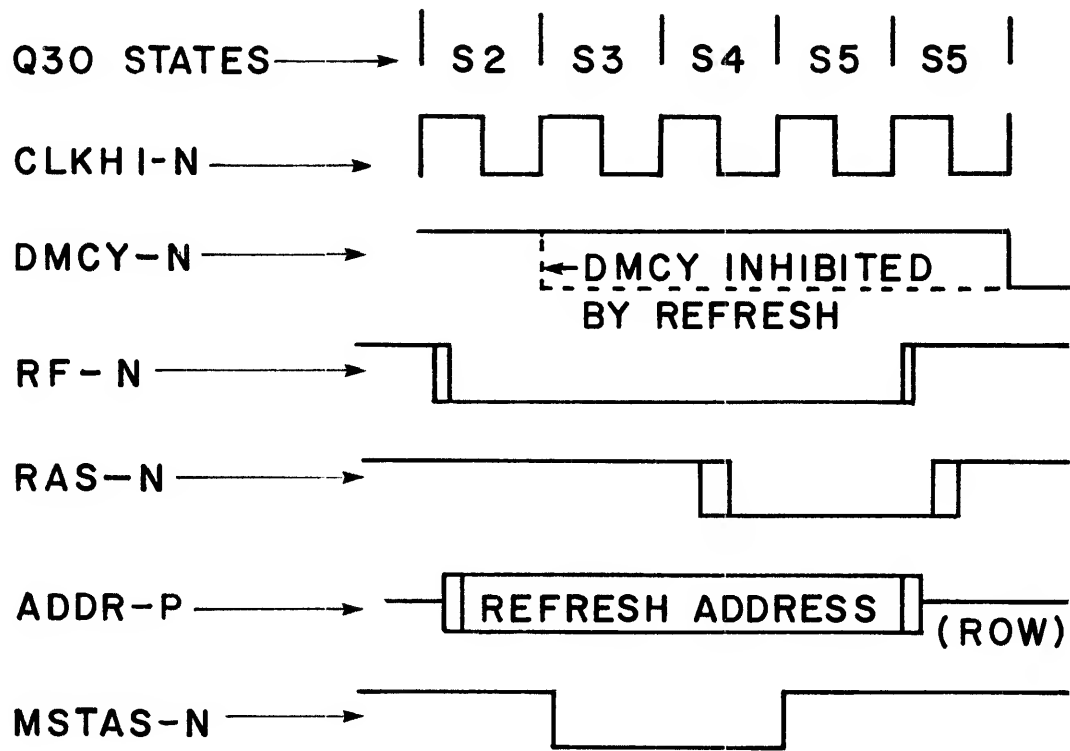
## READ CYCLE

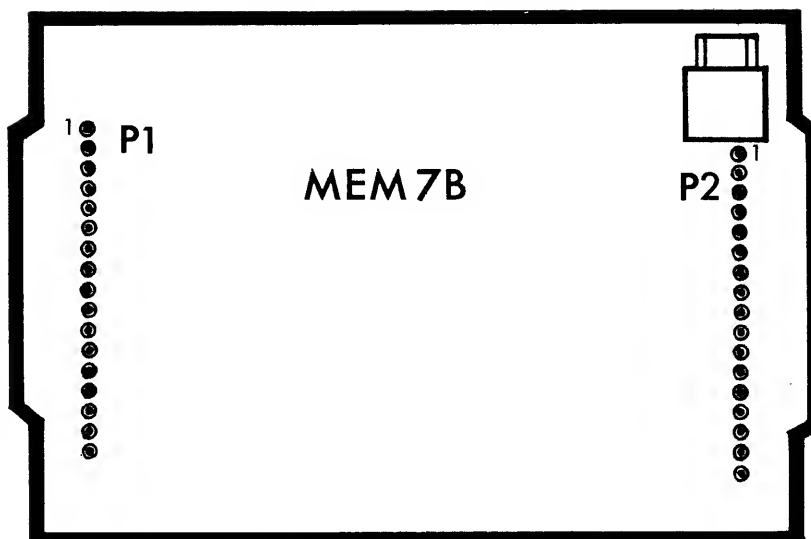


## WRITE CYCLE



## REFRESH CYCLE

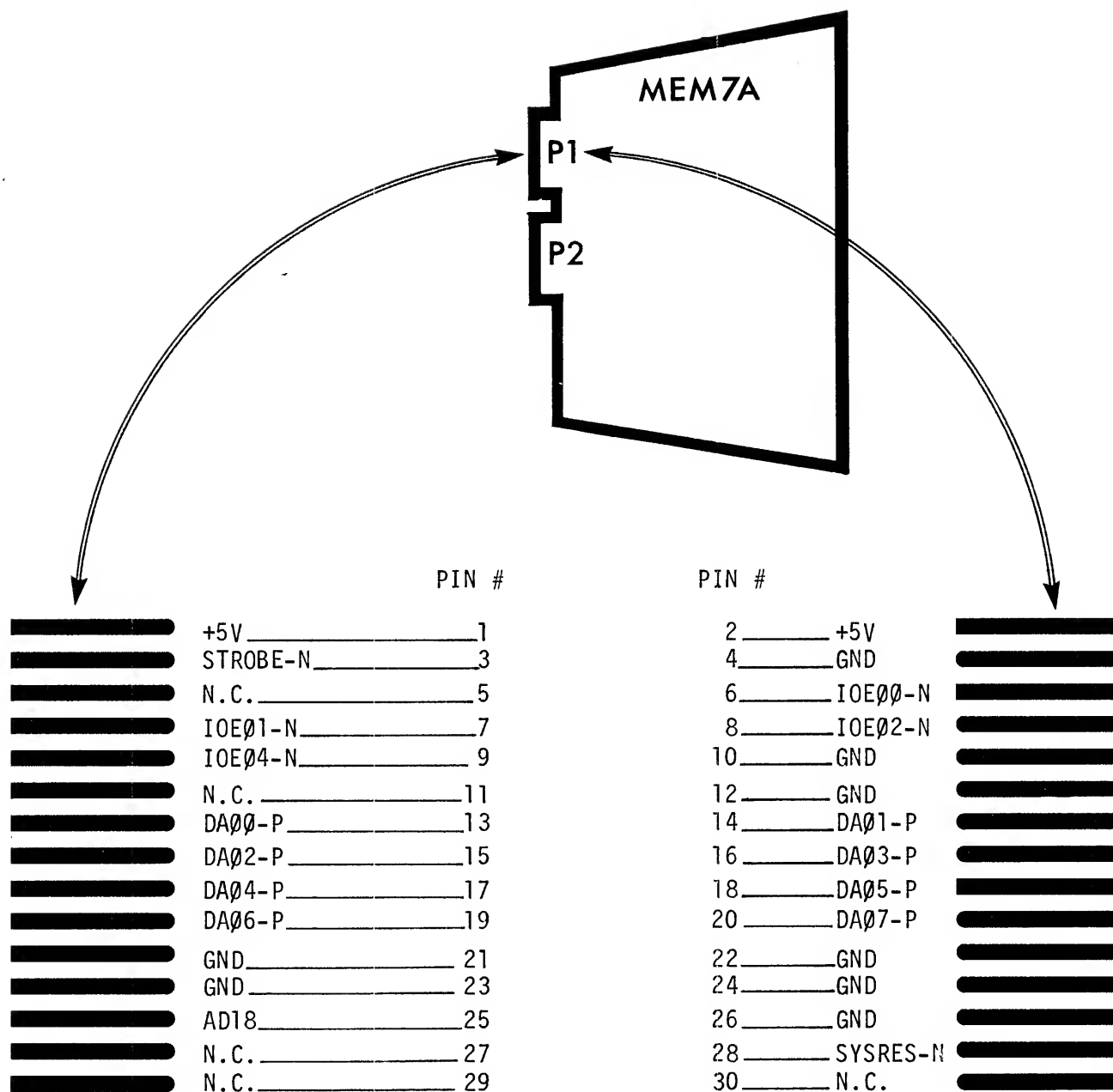


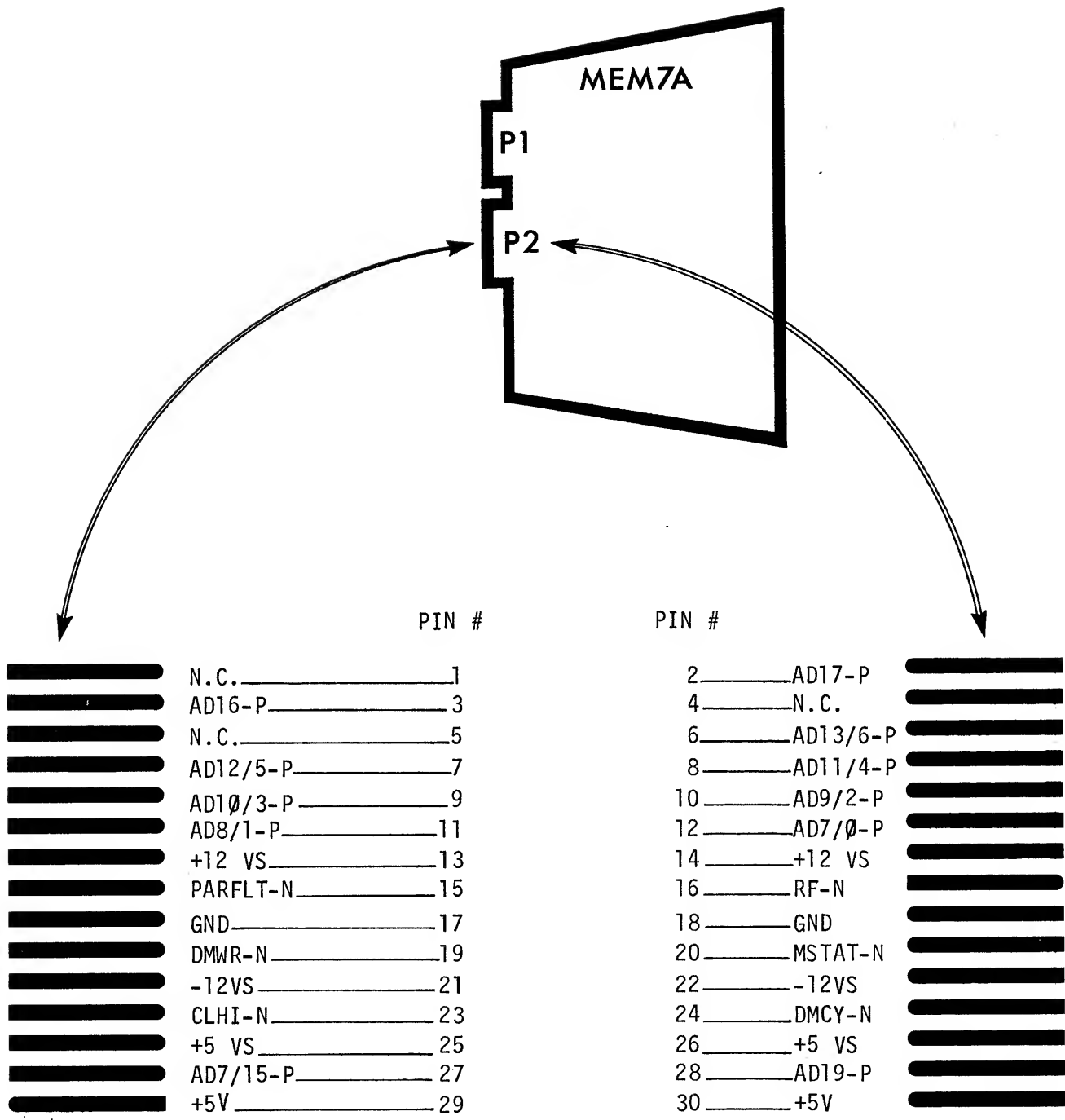


PIN # P1

PIN # P2

1. GND	1. +5V
2. +12V (not used)	2. KEY
3. KEY	3. SETIND-N
4. CAS-N	4. DB02-P
5. WRT-N	5. DB01-P
6. RASA-N	6. DB00-P
7. MA06-P	7. DB03-P
8. MA00-P	8. DB05-P
9. MA03-P	9. RASB-N
10. MA02-P	10. DB04-P
11. MA04-P	11. DB06-P
12. MA01-P	12. DB07-P
13. MA05-P	13. PD-P
14. -5V (not used)	14. +12VS
15. -5V (not used)	15. +12V (not used)
16. +5V	16. GND
17. MA07-P	17. Not Used





D32109-001

RAS-N (6A3, 4A5, 6D3)

WRD-N (6D2, 8A5)

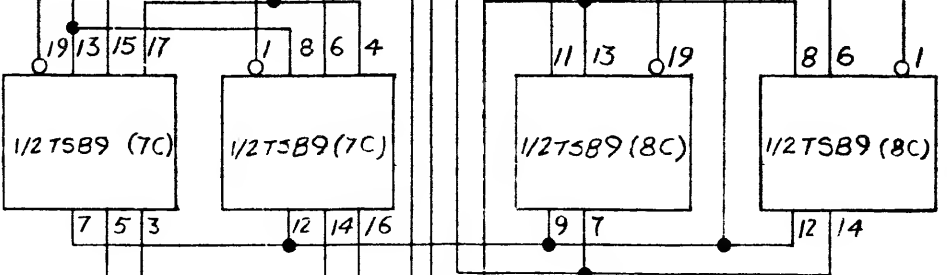
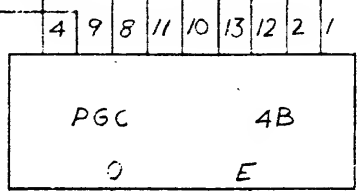
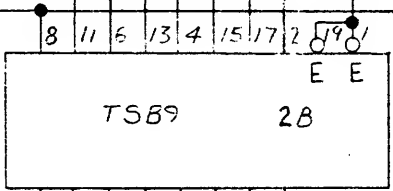
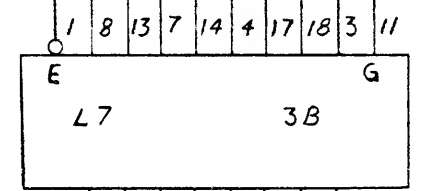
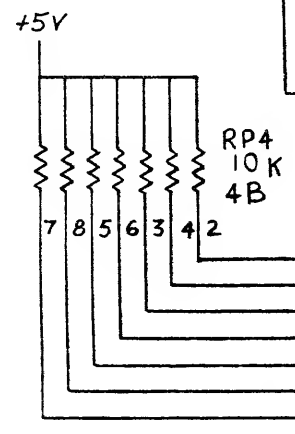
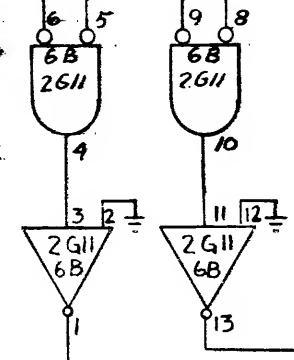
RDD-N (8D5)

DA07-P (8D7, 7A6)  
DA06-P (8D7, 7A6)  
DA05-P (8D7, 7A6)  
DA04-P (8D7, 7A6)  
DA03-P (8D7, 7A6)  
DA02-P (7A6)  
DA01-P (8D7, 7A6)  
DA00-P (8D7, 7A6)  
CAST-N (6D1, 5A5)

NWR-N (8D4)  
SELEVEN PAR-N (7D7)  
SWR-N (8D4)

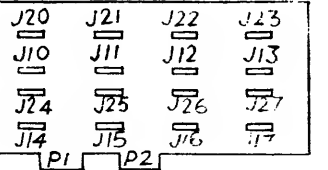
SRD-N (8D4)

NRD-N (8D3)

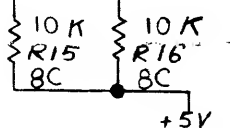


NOTES: UNLESS OTHERWISE SPECIFIED  
1. ALL RESISTORS IN OHMS, 1/4W, 5%.  
2. CAPACITANCE IN MICRO-FARADS.  
3. I.C.'S WHICH USE +5VS WILL BE SO NOTED. ALL OTHER I.C.'S USE STANDARD +5V.

J20, J21, J22, J23, J24  
J25, J26, J27  
DB07-P  
DB06-P  
DB05-P  
DB04-P  
DB03-P  
DB02-P  
DB01-P



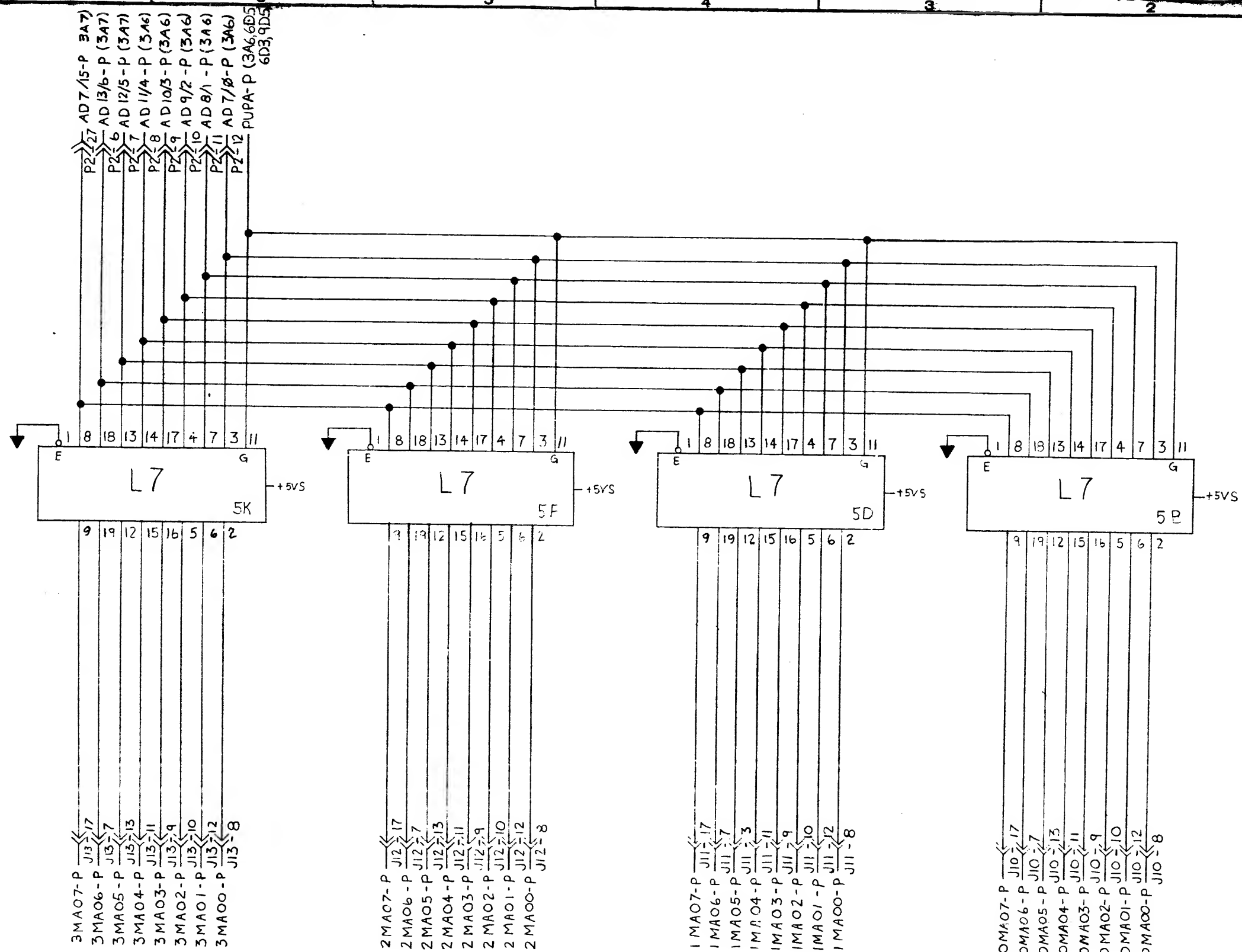
J20, J21  
J22, J23  
J24, J25  
J26, J27  
FD-P  
-6  
-13



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TITLE		LOGIC, MEM 7A	
DWN. 1/2/82		SHEET 1 OF 9	
END. 1/2/82		DRAWING NO. D32109-001	
PROG. 1/2/82		ISSUE	
REV. 1/2/82		C	
RELEASE DATE 7-15-82			

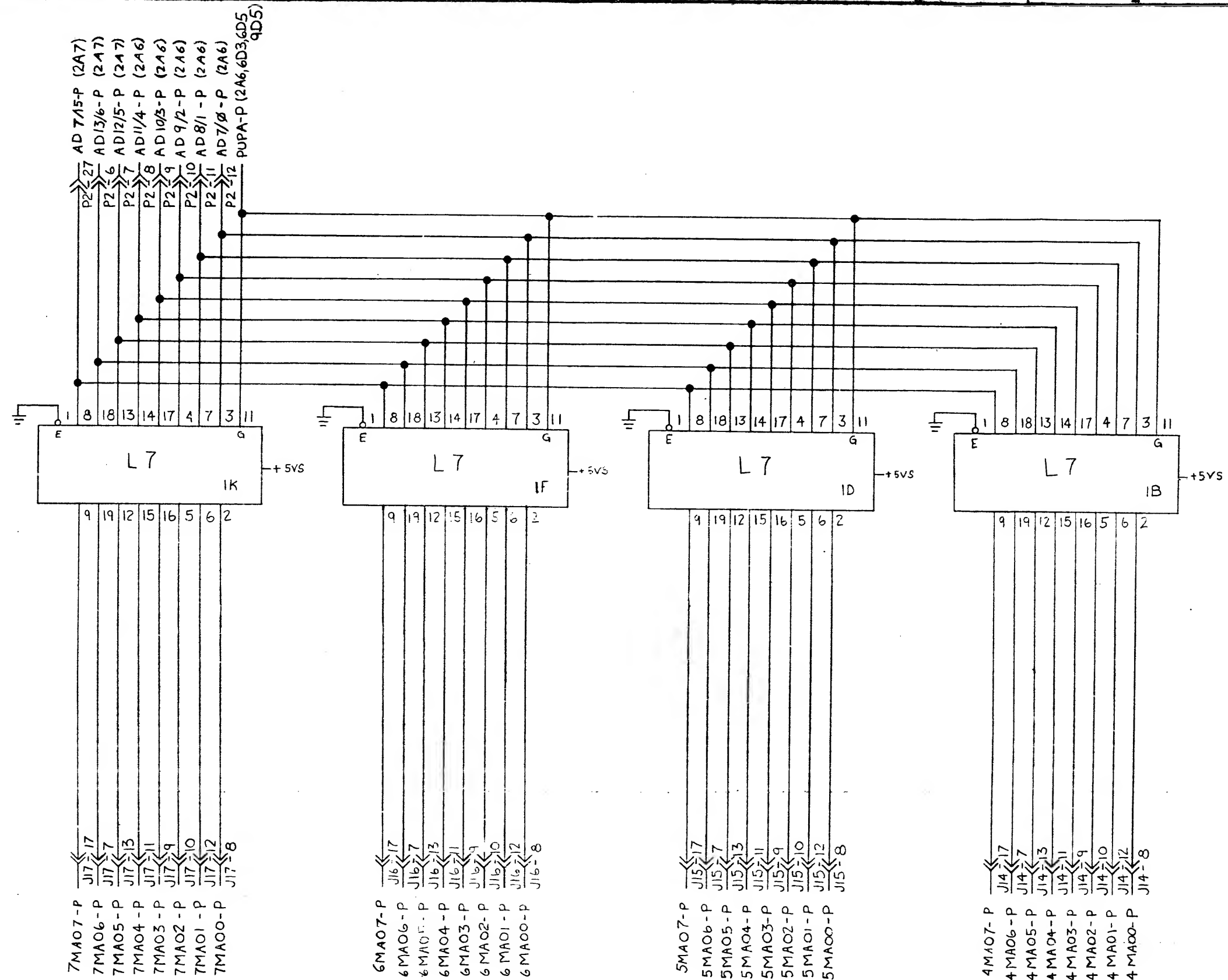
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CHK: 1/2/82	
APPD: 1/2/82	
REVISED PERSON	
ECN: 3664	
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REVISED PERSON	

"PRODUCTION RELEASE"



D32109-001

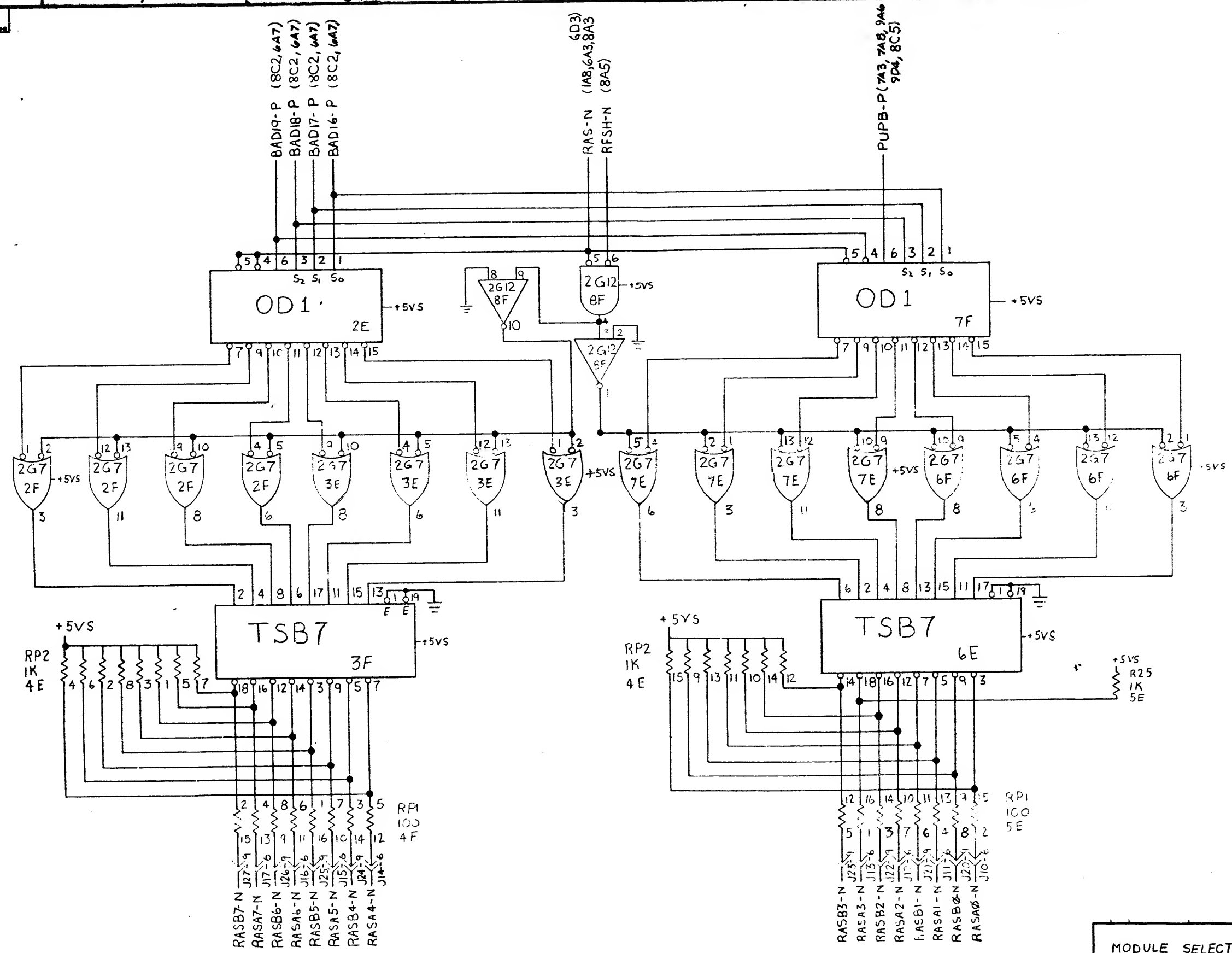
REVISIONS	
DATE	BY
	A
	B
	C



ADDRESS LATCHES		<b>MDS QANTEL</b> <small>A Micro Data Storage Company</small> 4140 POINT BURN WAY • HAYWARD, CALIF. 94505	
TITLE		LOGIC MEM 7A	
DWN. 7 CRUZ PM 88	END.	SHEET 3 OF 9	DRAWING NO. D32109-001
RELEASE DATE 7-15-82	APP. 3	ISSUE C	

100-601220

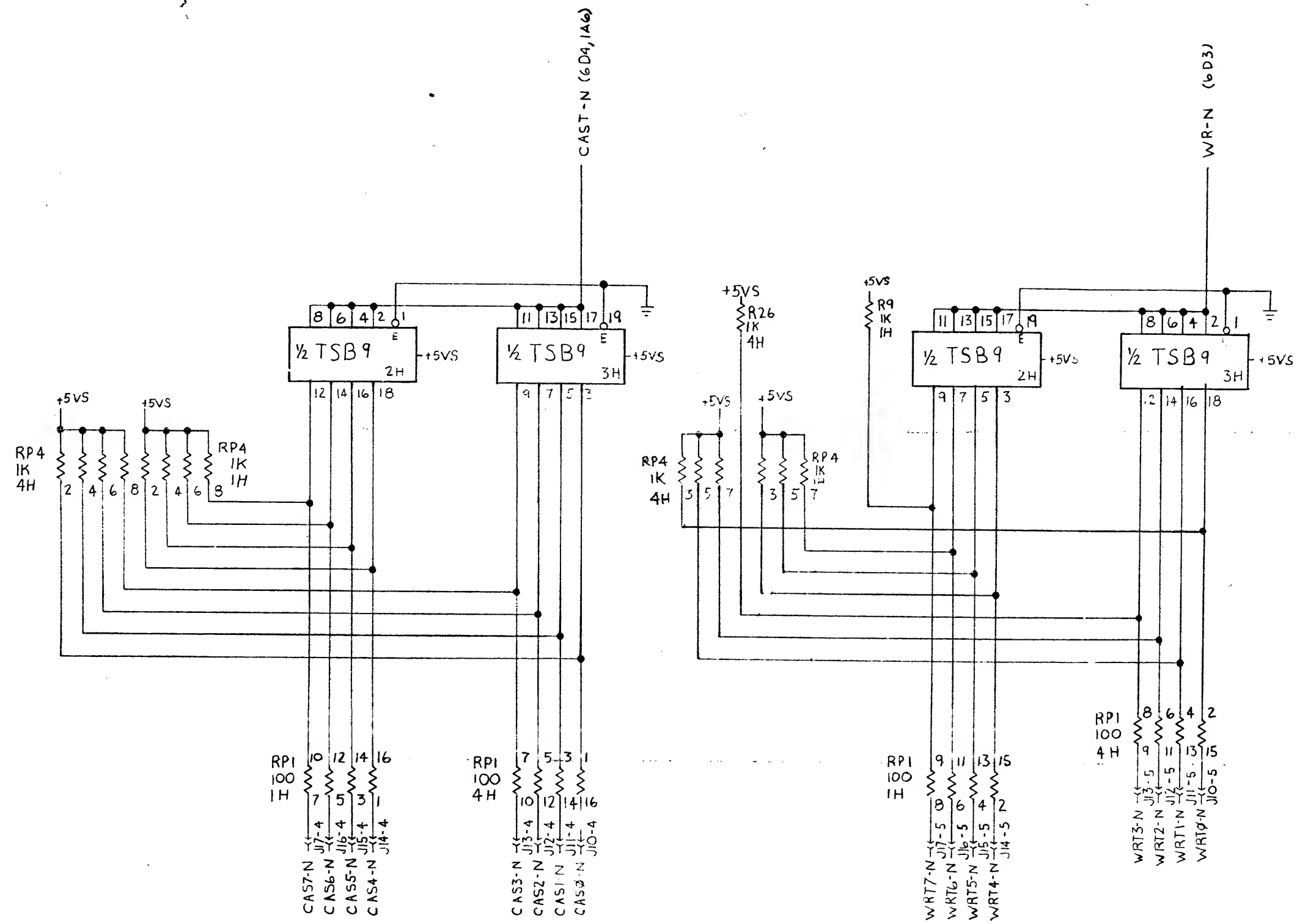
REVISIONS	
DATE	BY
	A
	B
	C



MODULE SELECT		MDS QANTEL	
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		SHEET 4 OF 9	
		DRAWING NO. 032109-001	
RELEASE DATE 7-15-82		DATE	

D32109-001

REVIEWS	
DATE	ISSUE
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	B
	C

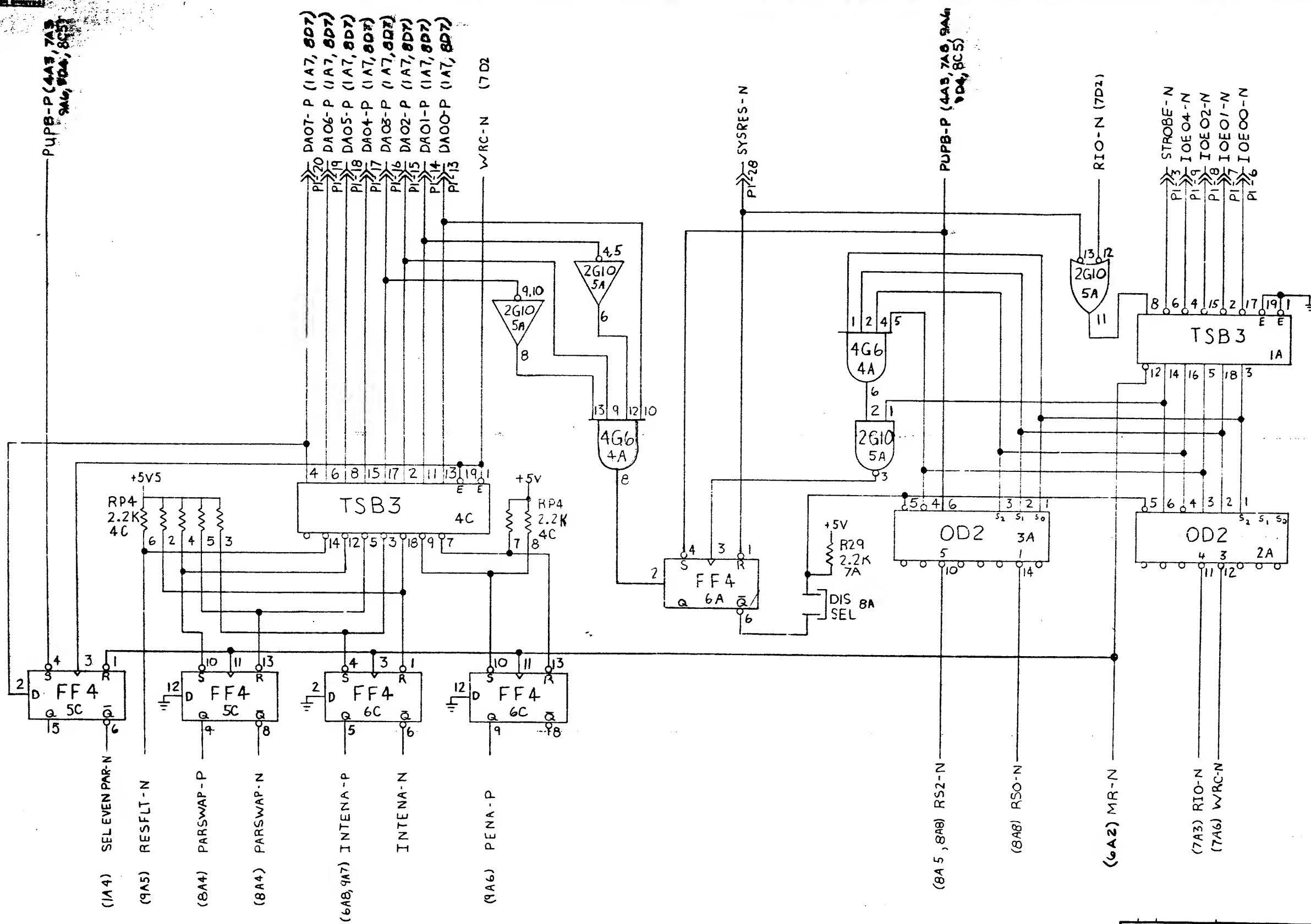


CLOCK BUFFERS		<b>MDS QANTEL</b> A Memory Data Systems Company 5140 POINT BURN WAY • HAYWARD, CALIF. 94545	
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RELEASE DATE 7-15-82		DRAWING NO. D32109-001	

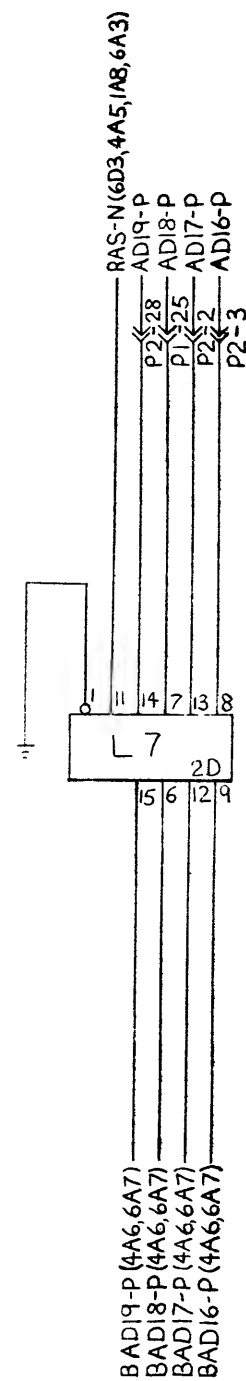
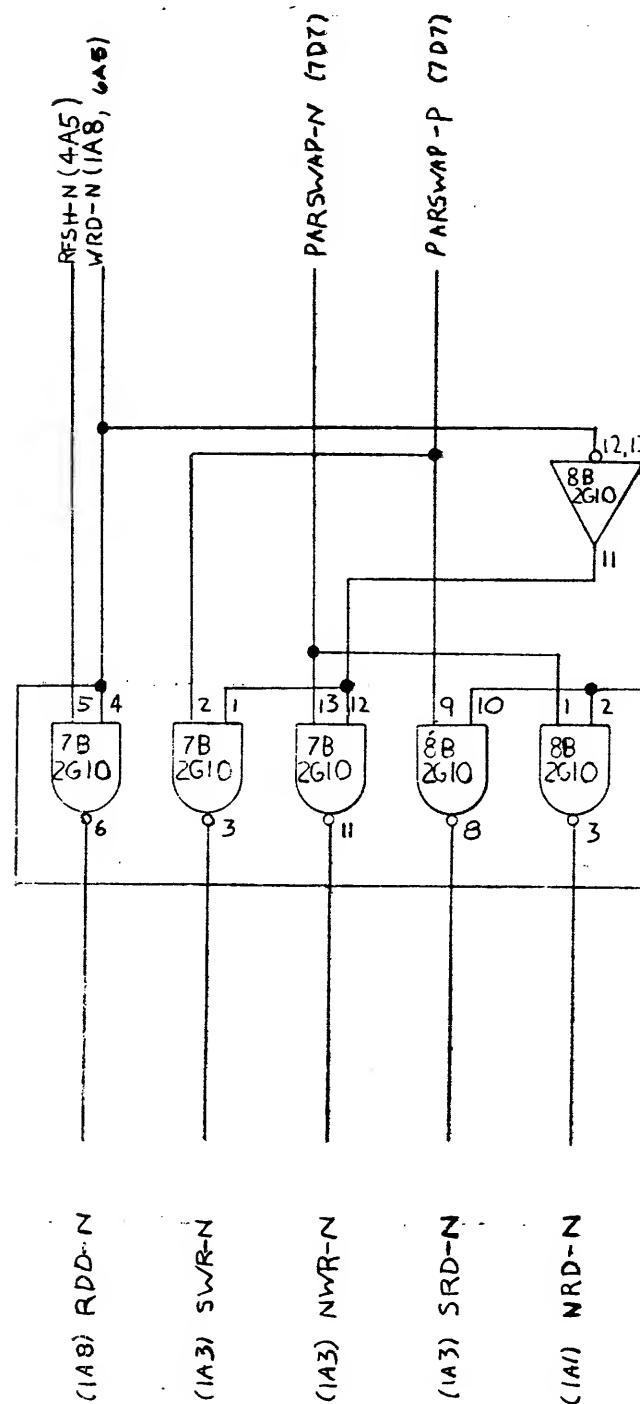
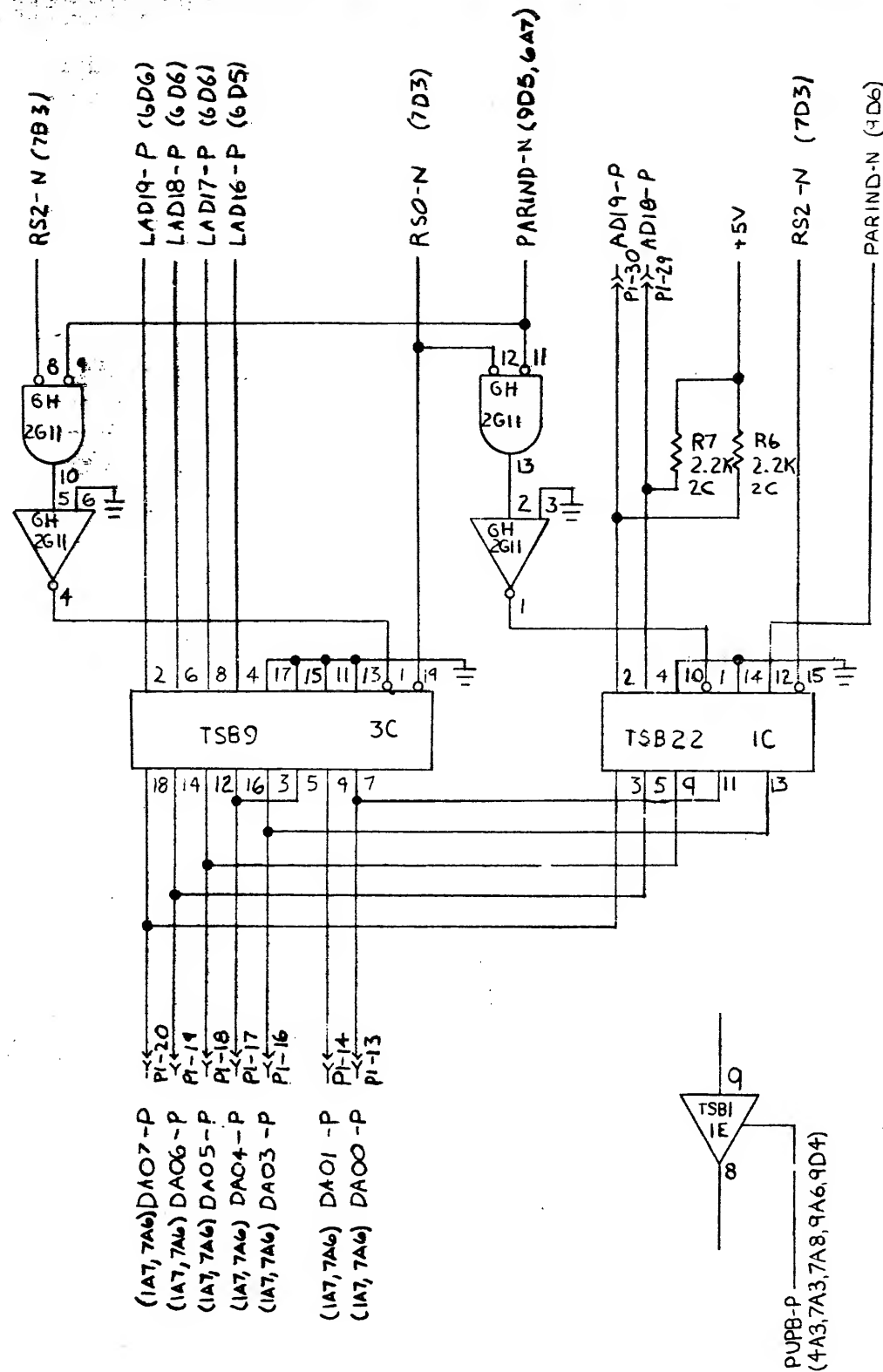


100-6012ED

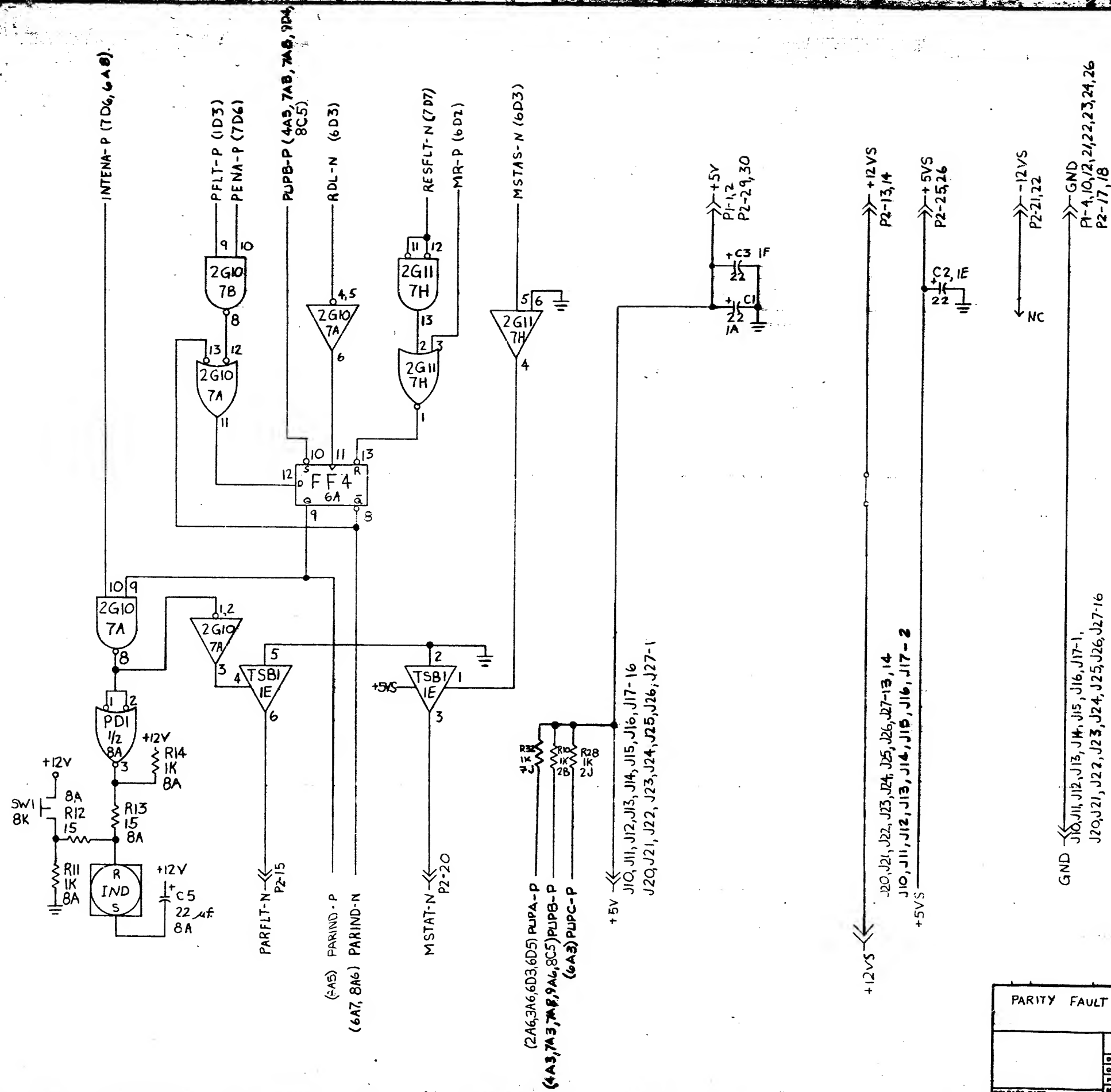
PUPB-P (4A3, 7A3, 9A6, 8D4, 8C5)



SELECT FLIP-FLOP & WRITE CONTROLS		<b>NDS QANTEL</b> A NDS Data Systems Company 4140 FIRST AVE. S.W. • HAYWARD, CALIF. 94541	
TITLE <b>LOGIC MEM 7A</b>		DRAWN: J. K. B. & M. B. CHKD: PROD: MFR: ENG: 7-15-72	
RELEASE DATE 7-15-72		DRAWING NO. 7 OF 9 D32109-001	



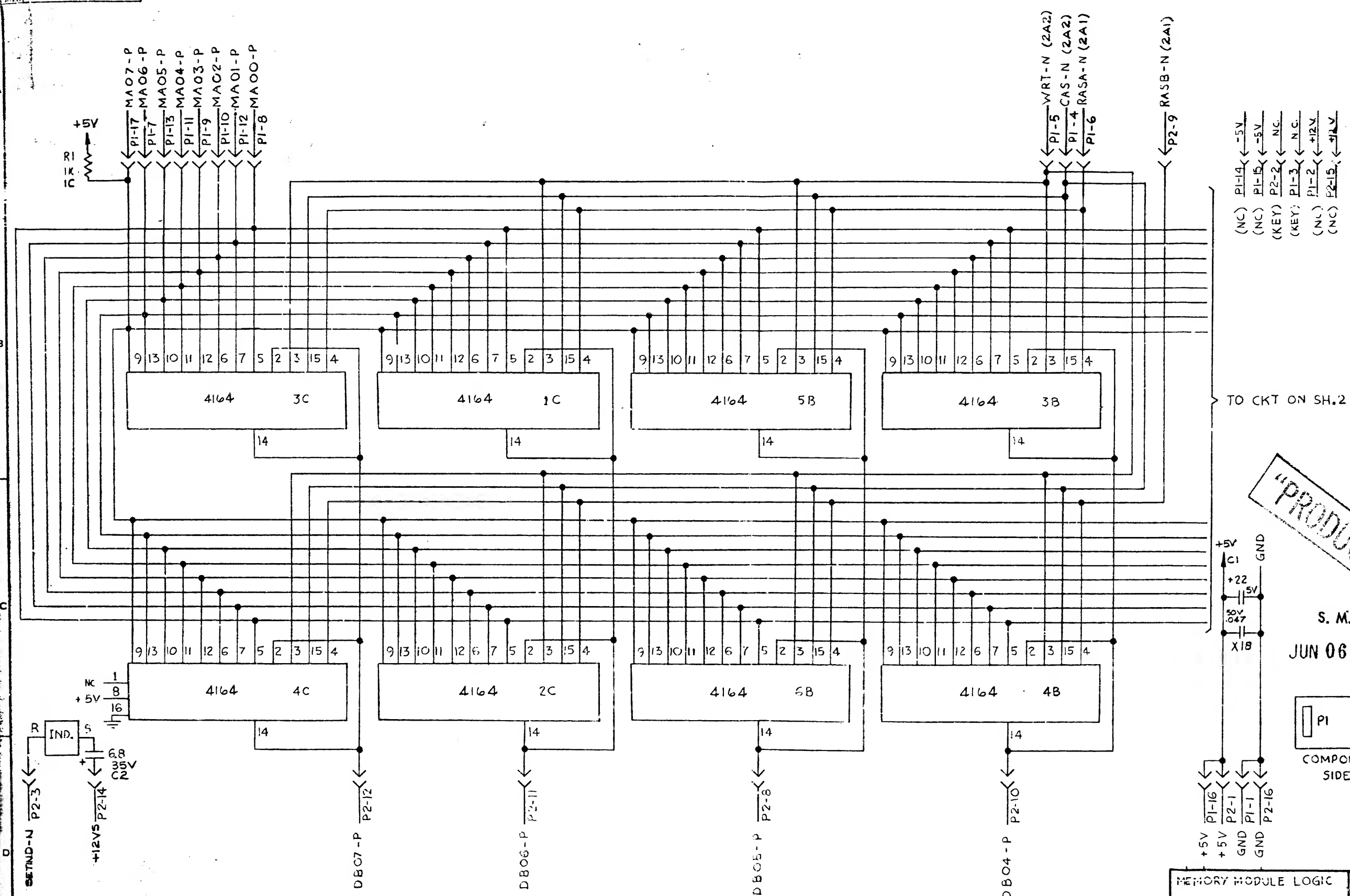
STATUS OUT & MODE SELECT		NDS	
RELEASE DATE 7-15-82		LOGIC MEM 7A	
8 of 9		D32109-001	



PARITY FAULT STATUS		NDS	
TITLE		LOGIC MEM7A	
DATE	1/15/62	DATE	1/15/62
TIME	9:09	TIME	9:09
RELEASE DATE		D32109-000	

100-01129D

REVISIONS	
DATE	ISSUE
FR 11682-01	A
DWN: W.P.	
REVISED PER	B
ECN: 3608 P2-2	
DWN: W.P.	
CHG: 24 MAR 1983	
APP: DLS	



2. ALL RESISTORS VALUES ARE IN OHMS AND ARE 1/4 W, 5%  
1. ALL CAPACITOR VALUES GIVEN IN MICRO-FARAD, VDC.  
NOTES: UNLESS OTHERWISE SPECIFIED

MEMORY MODULE LOGIC

RELEASE DATE

7-15-92

**MDS**  
MICRO DATA SYSTEMS  
A MICROSAT DATA SYSTEMS COMPANY  
4148 PORT EDEN WAY, HAYWARD, CALIF. 94542

TITLE

LOGIC, MEM. 7B

SHEET

1 OF 2

DRAWING NO.

D32110-001

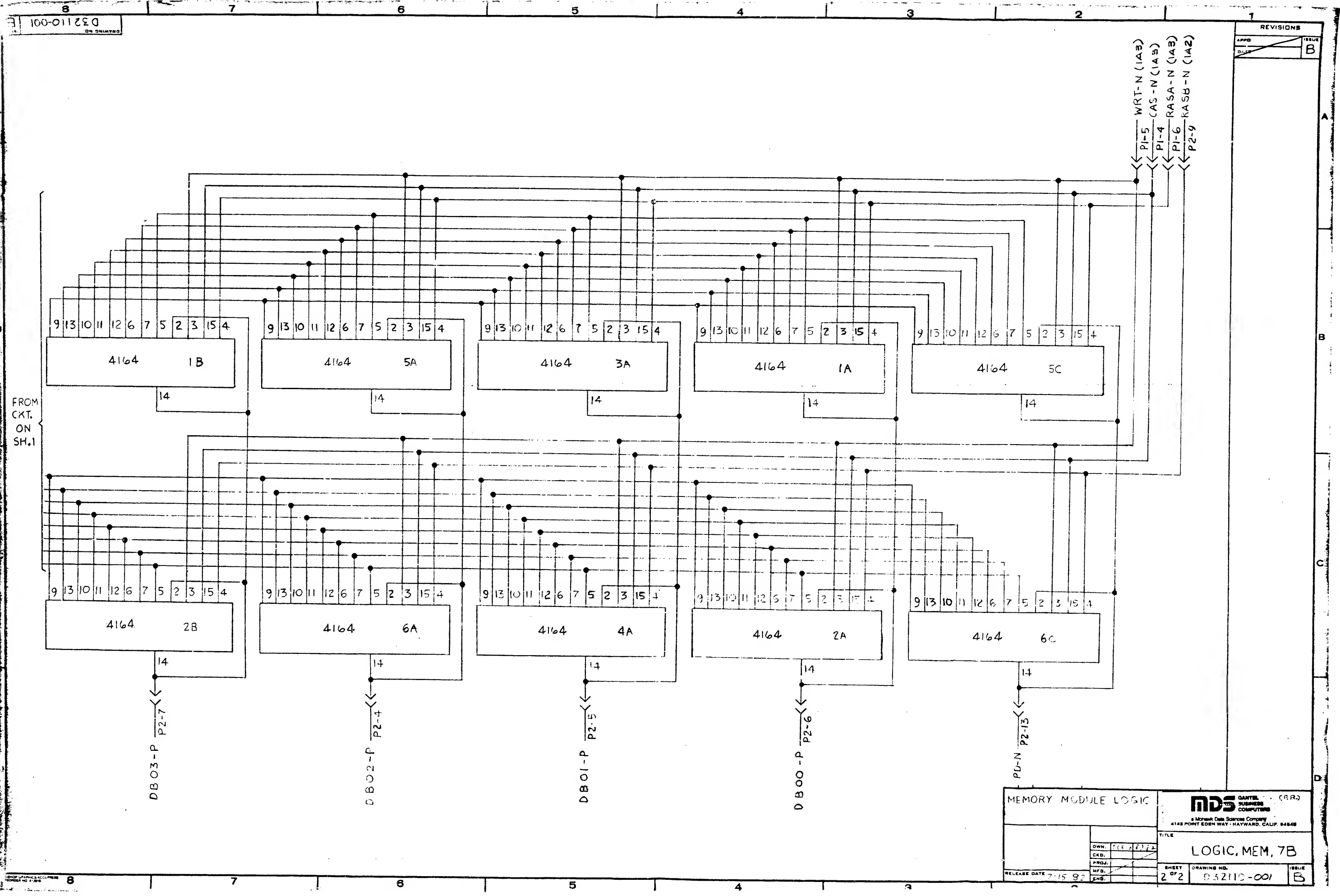
ISSUE

B

"PRODUCTION RELEASE"

S. M.  
JUN 06 1983

COMPONENT SIDE



MEMORY MODULE LOGIC		MDS GANTHE (C.R.) BUSINESS COMPUTING 4142 POINT EDEN WAY, HAYWARD, CALIF. 94542	
OWN. T.C.C. 6/2/72	CKD. 6/2/72	TITLE LOGIC, MEM, 7B	
PROJ.	ENG.	SHEET 2 OF 2	DRAWING NO. 032110-001
RELEASE DATE 7-15-82		ISSUE B	